Synopsys Interoperability Breakfast
43rd Design Automation Conference
July 26, 2006

Escape from "Analog Alcatraz" Through OpenAccess

Jim Hogan

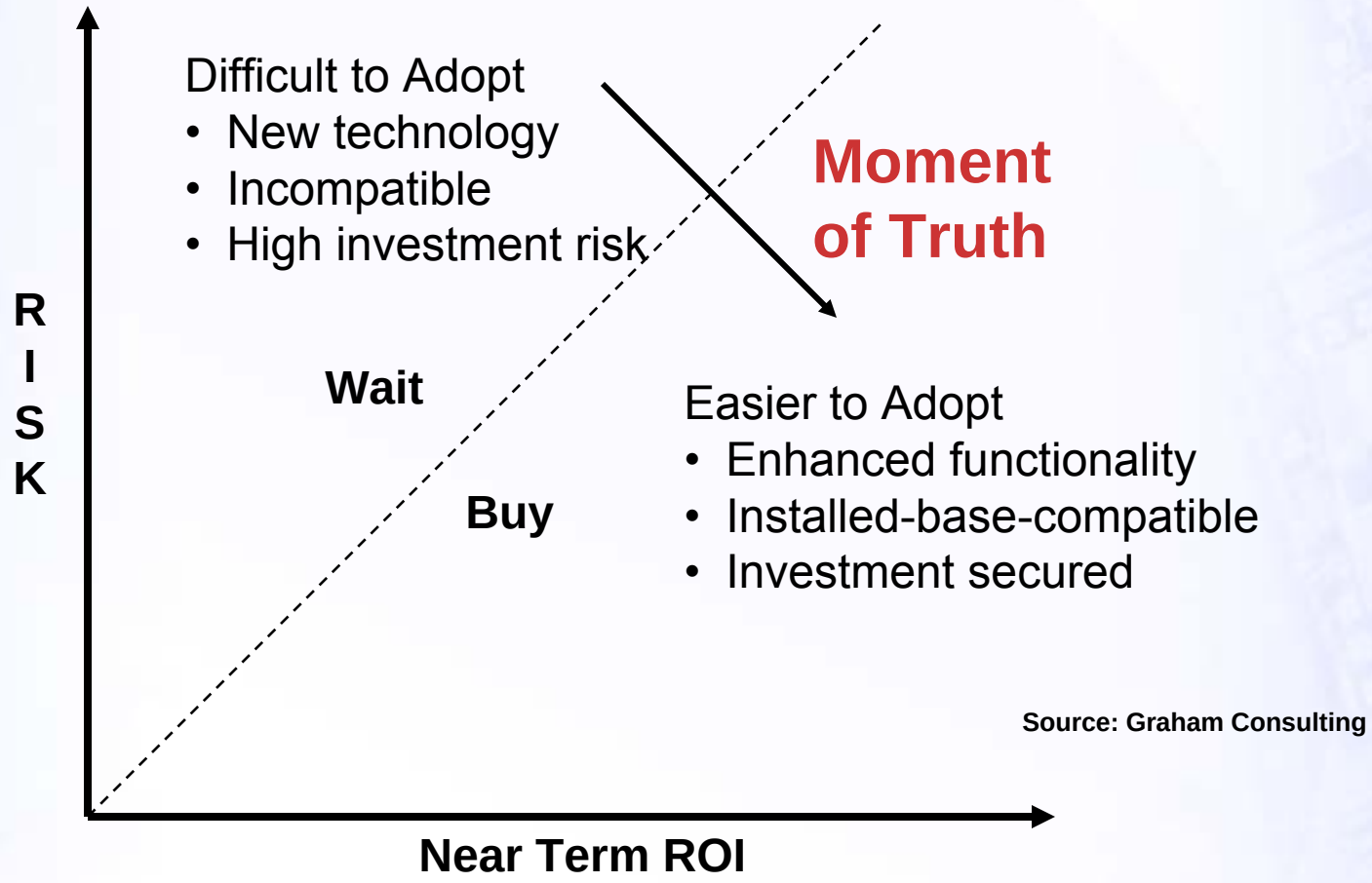
Why Openness?

- Enhance the value of an architecture franchise:
  - TI DSP, Intel PCI/PCI Express, ARM's wireless platform, etc.
  - Stable and predictable roadmaps lead to long-term investment
  - Overall growth through complementary products
  - Expanded reliance on the virtual supply chain or eco-system
- Directly address pent-up consumer demand
  - Better functionality, cost, ease-of-use
  - Better integration with existing devices, systems

Why Openness?

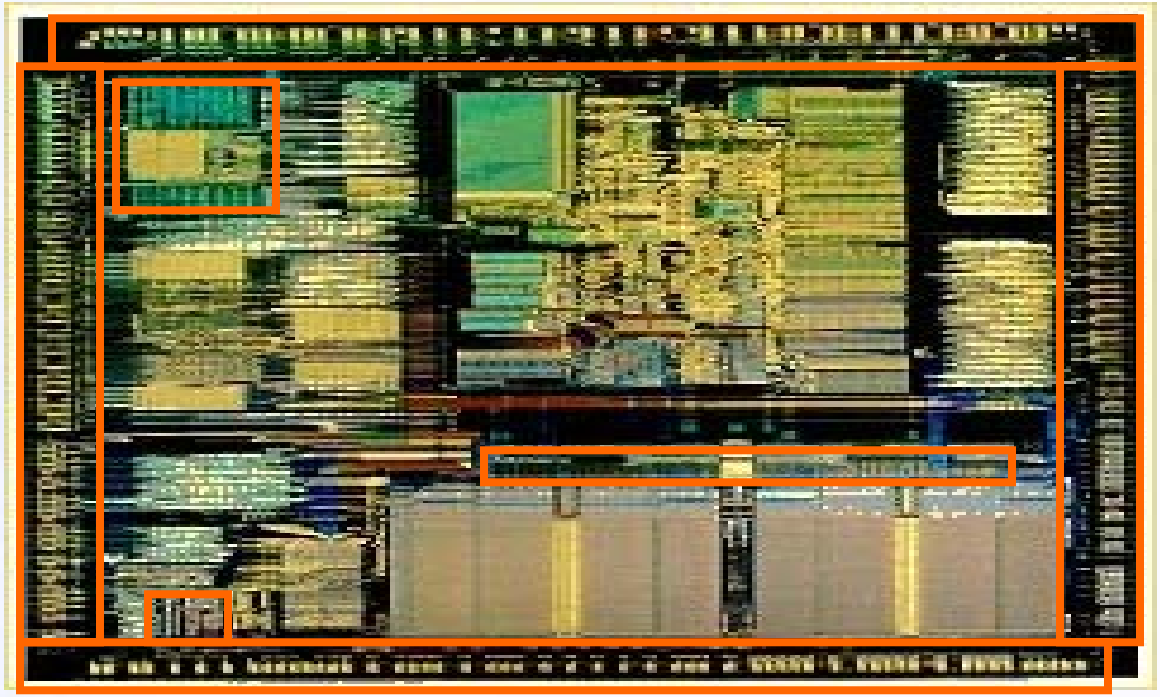
- Openness expands markets and value creation of tools by:
  - Reducing the cost of vendor entry
    - ◊ Application software, Channel
  - Spreading the risk of innovation (HTML, CDMA/GSM)
    - ◊ Allows start-ups to focus on their differentiating technologies
    - ◊ Lowers the cost of market access
  - Accelerating consumer choice (DVD, CD, MP3)
  - Rapid opening of adjacent markets (WiFi 802.11b/g/n)

Economics of Openness



Source: Graham Consulting

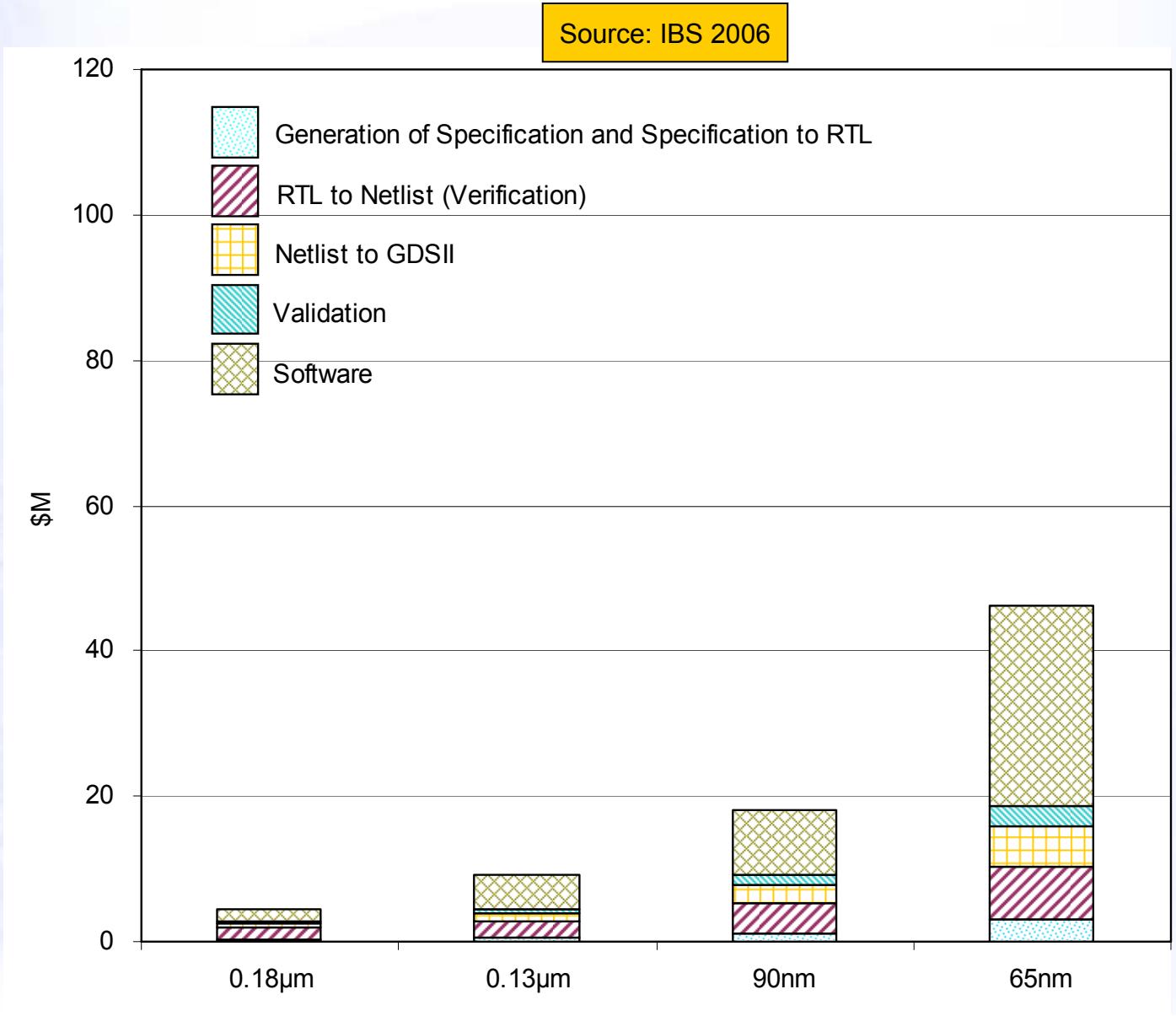
SoC Snapshot: Analog Custom is the Value-added IP



- **Today's SoCs:**
  - **Have tens of millions of digital gates, however …**
  - **Every SoC has many analog and mixed-signal elements,**
  - **Many of them third-party IP**
  - **Just as with board-level components, IP is selected via specification**

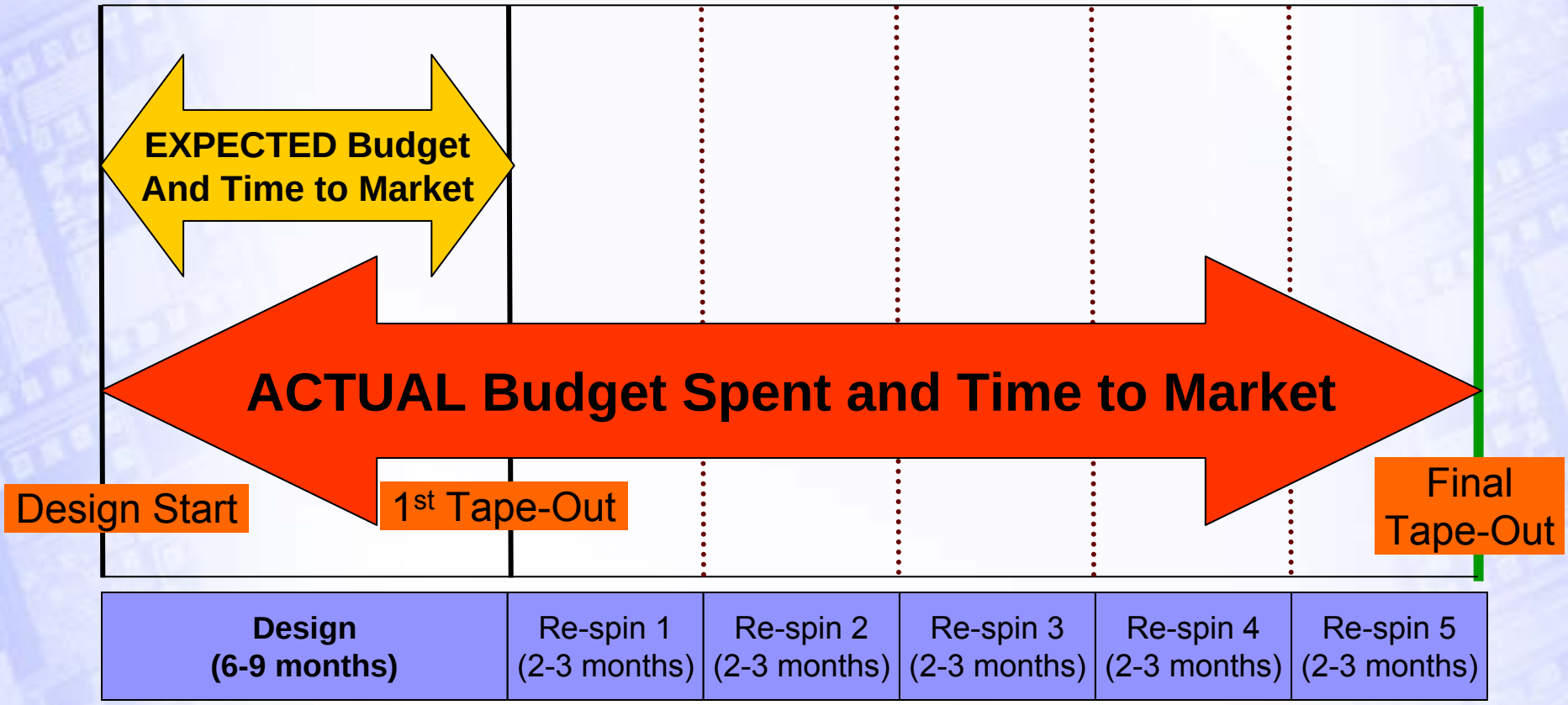
The analog and mixed-signal elements are <u>crucial</u> to today's SoCs.

DESIGN COST FOR ANALOG: A TYPICAL DESIGN

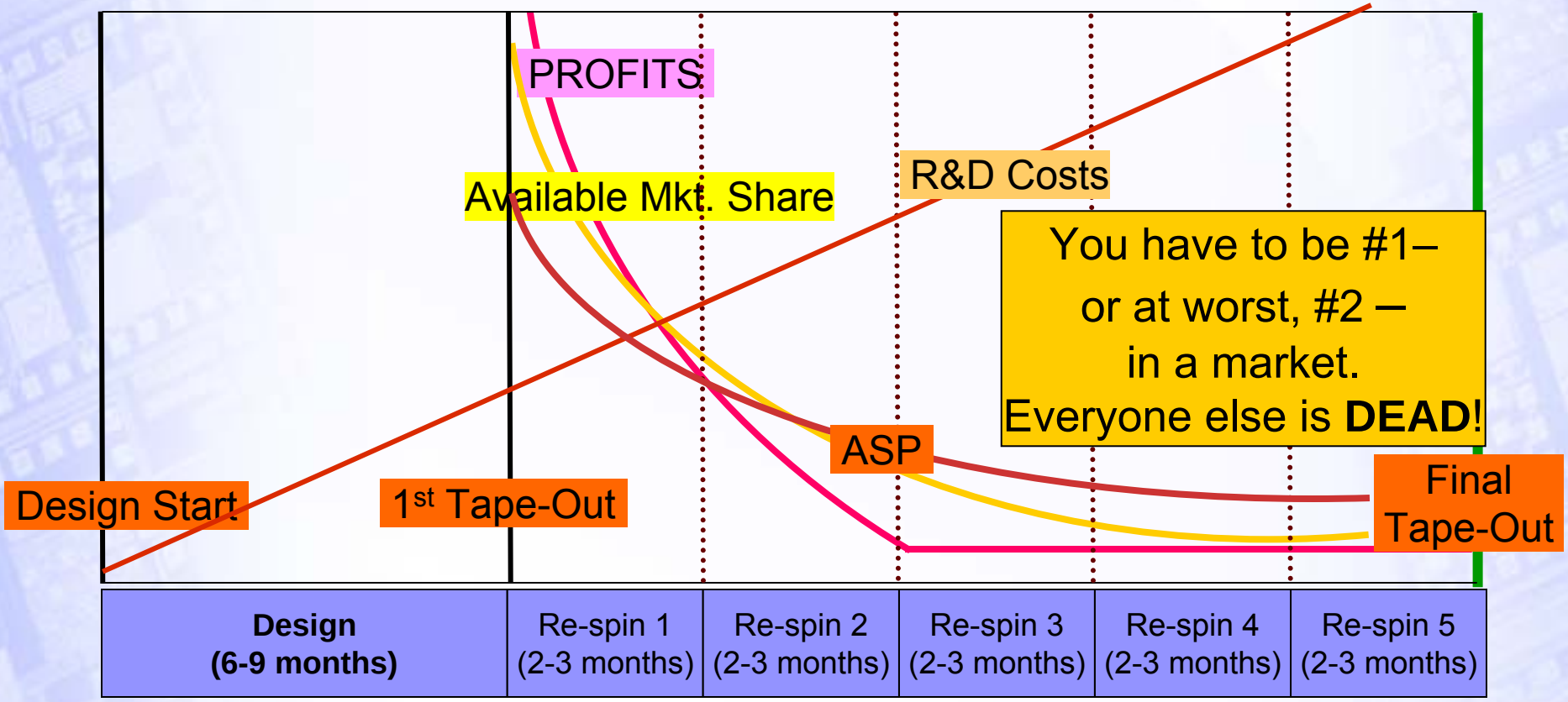


Jim Hogan, DAC 2006

Today's Reality

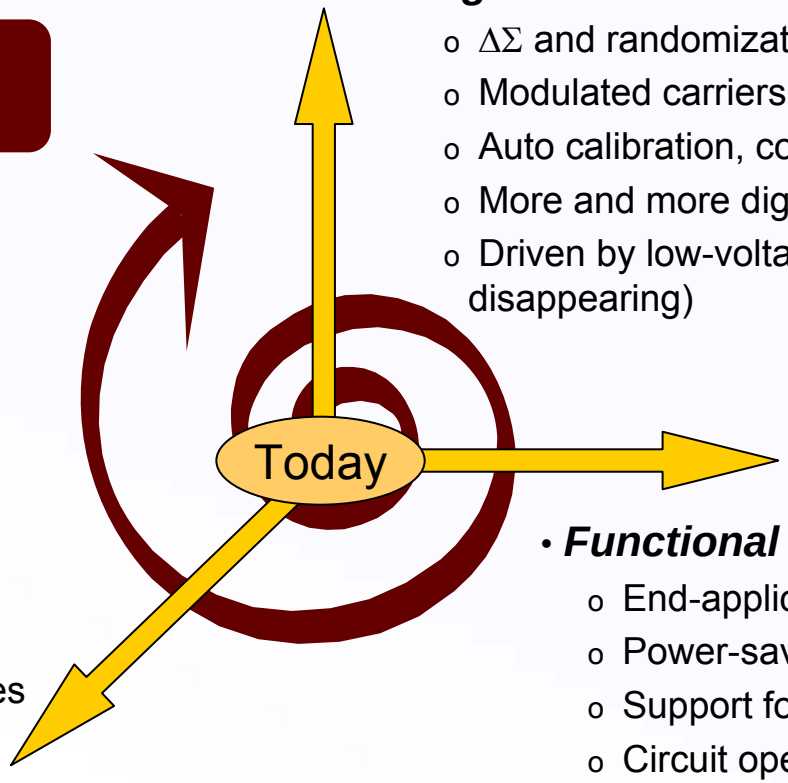


Economics: Typical Analog Design Project



Why Now? Exploding Analog Complexity!

Each dimension feeds the others



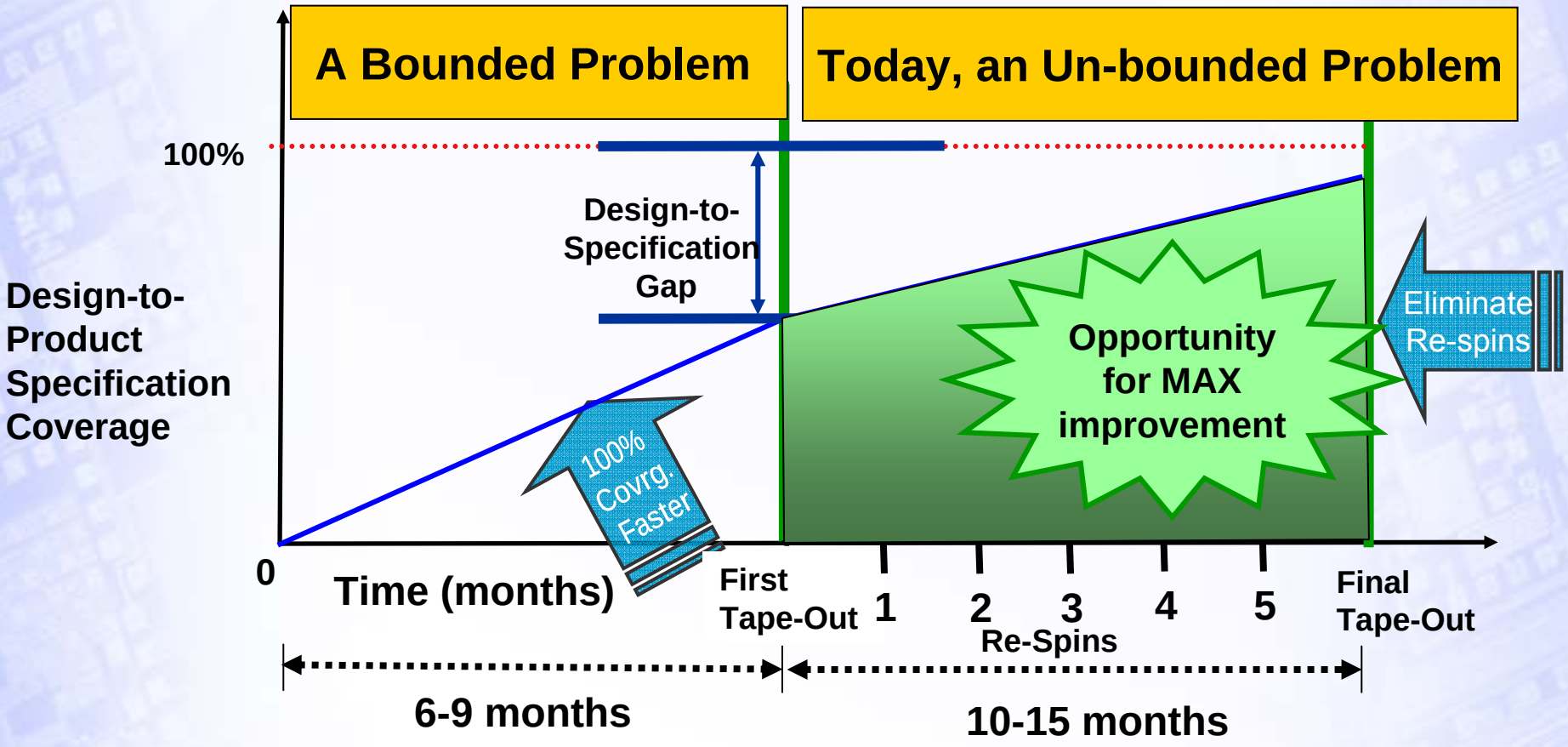
- ***Algorithmic Architectures***
  - ΔΣ and randomization
  - Modulated carriers
  - Auto calibration, correction, and adaptation
  - More and more digital controls
  - Driven by low-voltage design (topologies disappearing)

- ***Team Complexity***
  - Teams of more than 5
  - Geographically dispersed
  - Designers have different roles
  - Complexity of project management
  - Complex communications

- ***Functional Modes***
  - End-application modes
  - Power-saving modes
  - Support for worldwide standards
  - Circuit operation modes
  - Calibration/tuning for process variability
  - Testability modes

[Source: Designers' Guide Consulting. www.designers-guide.com]

How to Realize the Value? Separate the 'What' and 'How'!



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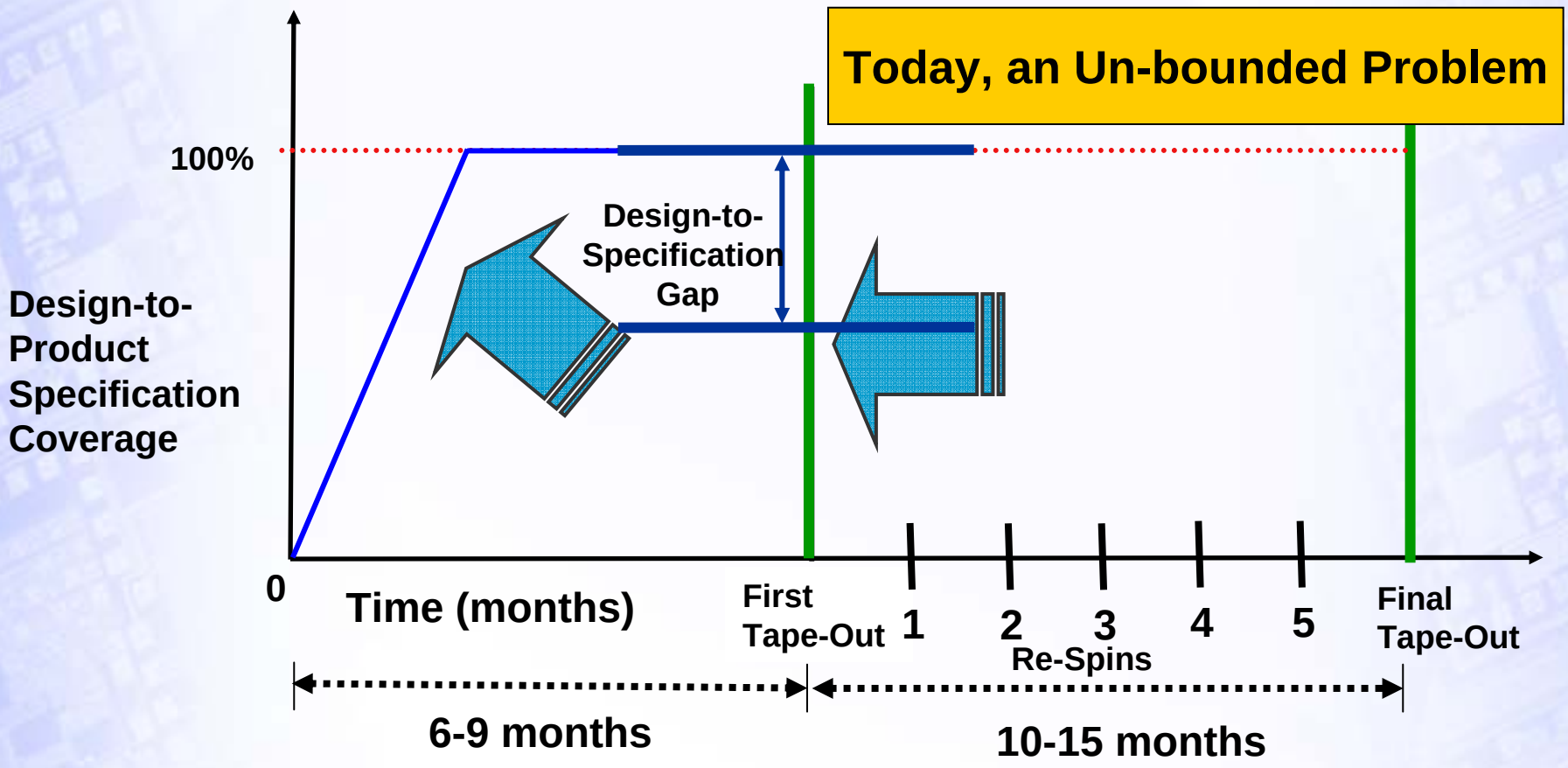
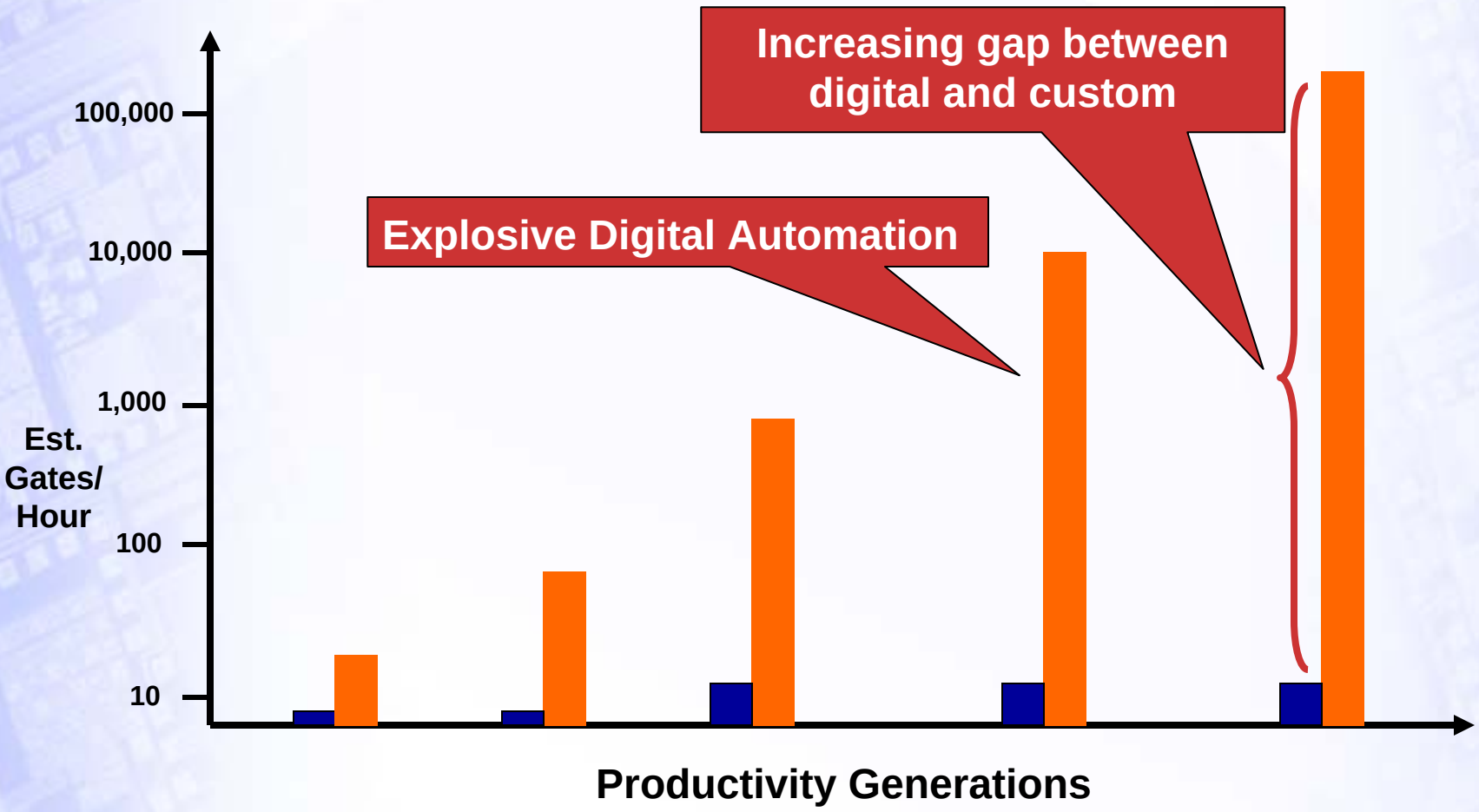


Analog Design, Both Electrical and Physical, is Under-Served

Need: Significantly Improved Efficiency and Productivity of AMS Design Teams



Digital Flow:	Schematic	Synthesis	3rd Party IP	1st Intg. Flow	Virtual Proto
Analog Flow:	Schematic	SPICE	PCells	No Change	No Change

A Good Place to Start: The Analog PDKs and PCells

- Process Design Kits (PDKs) contain the analog building blocks and library furnished by fabs
- Si2 now supports the 'OK Initiative'
- At the core of PDKs are the Parameterized Cell (PCells)
- PCells are similar to standard cells in the digital design flow
- PCells are a fundamental building block for Analog automation

PCell Challenges

- PCells are built early in the process life
  - Before a process matures, and generally focused on test chips and memory devices
    - Lots of iterations in the rules
  - Generally are very conservative
- PCells are created by most major fabless design houses
  - Re-design of foundry PCells to achieve true performance
  - And design of new PCells to address specific needs
  - Both cause long cycle-time delay
- PCells support only one EDA vendor solution
  - No interoperability between EDA tools from different companies

What Do We Want From An Open PCell?

- It is process-transportable
- It works with many design tools
  - Any design tools that work on the OpenAccess database
- Can be used with traditional SKILL PCells
- Uses non-proprietary, open language: Tcl or Python
- Universal PCell and custom-layout-generator design environment
- Language-based methodology with interactive author and debug environment
- “Design Rule Correct-by-Construction” layout

How? Use a Open Source Infrastructure.

- Python
  - A dynamic, object-oriented language
  - Used successfully in thousands of business applications, many large and mission critical systems
  - Google's engineering infrastructure is on Python
  - Open source, with an active user community: www.python.org
- OpenAccess
  - Next-generation database
    - Source code donated to Si2 by Cadence
    - Open-standard data API and reference database provide true interoperability
  - All major EDA vendors are members of Si2's OpenAccess Coalition
    - Cadence, Magma, Mentor Graphics, Synopsys
  - Maintained by Si2 (www.si2.org)