UPF : THE Industry Standard for Low Power

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GM and VP

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Magma Design Automation

UPF is the New Industry Standard

Built from Silicon-proven Technologies

Technology donations to UPF TSC

- **Mentor**
  - External power configuration file for verification
- **Magma**
  - Power Management commands
- **Vast**
  - System level modeling methodology and format
- **Synopsys**
  - RTL constructs (Verilog and VHDL)
  - Power Management commands
  - Switching activity format – SAIF
- **TI**
  - Retention cell semantics
- **Atrenta, Synchronous DA**

UPF Participating Companies

- AMD
- ArchPro
- ARM
- Atrenta
- Azuro
- Cadence
- ChipVision
- FreeScale
- IBM
- Infineon
- Intel
- LCDM Eng
- LSI Logic
- Magma
- Mentor
- Nokia
- Nordic Semi
- Novas
- NXP
- Qualcomm
- Si2
- STARC
- STM
- Synchronous DA
- Synopsys
- TI
- Toshiba
- VaST
- Virage Logic
- Xilinx

- **Feb 07 – UPF 1.0 standard approved by Accellera !**
- **May 07 – IEEE P1801 Working Group underway**

UPF – Fast Response to Industry Need

Date	Milestone
11 Sep 06	Accellera TSC formation
18 Sep 06	Design Objectives Document; Weekly meetings start
5 Oct 06	Si2 / Accellera Workshop on Low Power
23 Jan 07	Accellera Technical committee approves standard
22 Feb 07	Accellera Board approves UPF – V1.0 released
23 Feb 07	IEEE study group formed
7 May 07	P1801 Low Power IEEE Working Group Approved
15 Jun 07	Deadline to submit donations for consideration by P1801

Public Download http://www.accellera.org

UPF 1.0 Industry Endorsement & Support

- **Infineon** - The quick development and release of the UPF 1.0 standard is based on our close partnership relations with EDA suppliers who share the same vision and attitude in making things happen. We are convinced that UPF will support us in achieving zero-defect quality and our productivity objectives, which both are key for Infineon's World class Automotive Product Portfolio.

  Hartmut Hiller, Senior Director Design Methodology Automotive, Industrial & Multimarket

- **Synopsys** - Applauds Accellera for approving the UPF standard for low power design and verification. We plan to deliver our UPF 1.0-based implementation and verification solution during 2007. In response to customer demand for a standard that enables consistent and interoperable end-user low power flows and methodologies, Synopsys - together with Magma Design Automation, Mentor Graphics, leading end-customers and IP companies - has made strong contributions to UPF 1.0 based on our proven technologies. UPF 1.0 is ready for industry use.

  Rich Goldman, Vice President, Synopsys, Strategic Market Development

UPF 1.0 Industry Endorsement & Support

- **Magma -** The speed at which the UPF standard has been developed and approved demonstrates the power of one open, inclusive and cooperative industry-wide effort. Users will realize significant improvements in productivity and quality of results by having a single, portable file and format with which they can specify, modify and maintain design data. Accellera, Magma, Mentor, Synopsys and all the companies that donated technology and expertise should be commended.

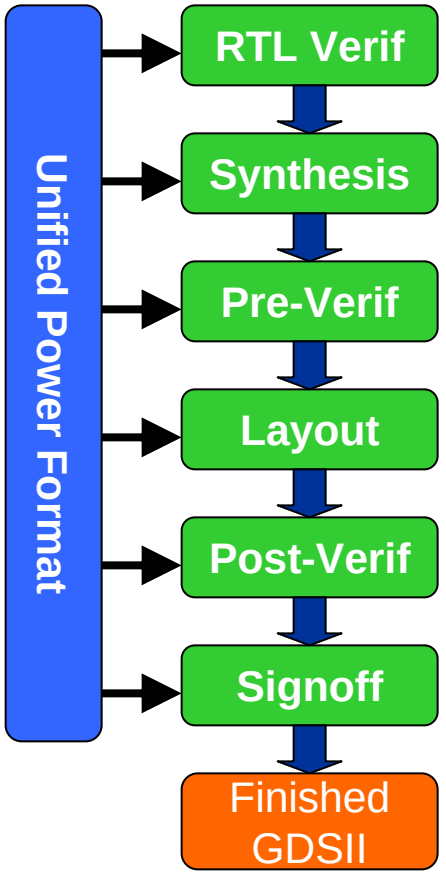
  Kam Kittrell, General Manager, Design Implementation Business Unit, Magma Design Automation

- **Mentor -** Designers want a single format that is simple to use, extensible, and capable of describing complex power behavior. The Unified Power Format (UPF) 1.0 standard achieves this by being open and comprehensive enabling support from leading EDA vendors and customers for industry-wide adoption. Mentor is committed to Accellera's UPF 1.0 standard as we are a leading contributor of our proven technology to this open standard for low power design and verification

  Robert Hum, Vice President & General Manager, Mentor Graphics Design Verification & Test Division

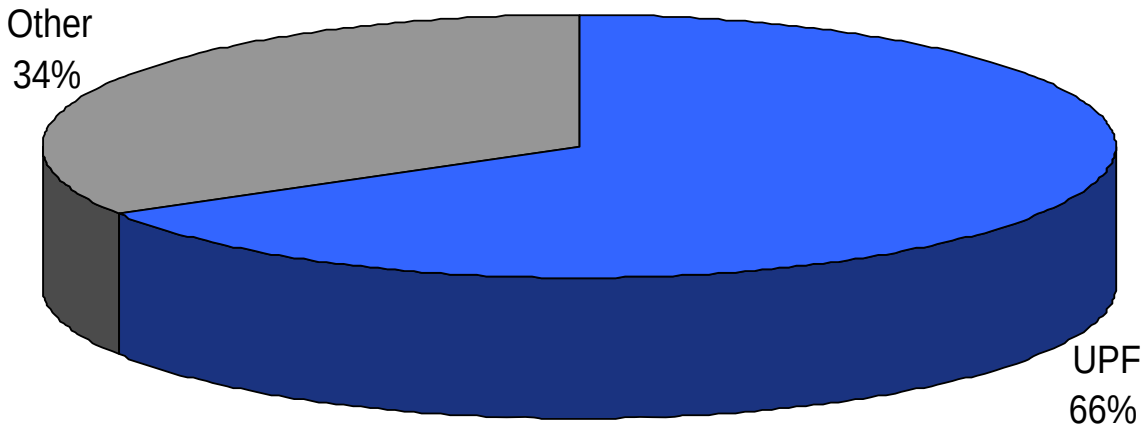
UPF Benefits

- **Productivity**
  - Same intent used for all throughout entire low power flow
  - Interoperability and productivity with mixed EDA flows
- **High Quality Results**
  - Consistent intent throughout flow = better checking and convergence
- **Simple IP Reuse**
  - Supports IP specification and use
  - No changes needed to golden HDL



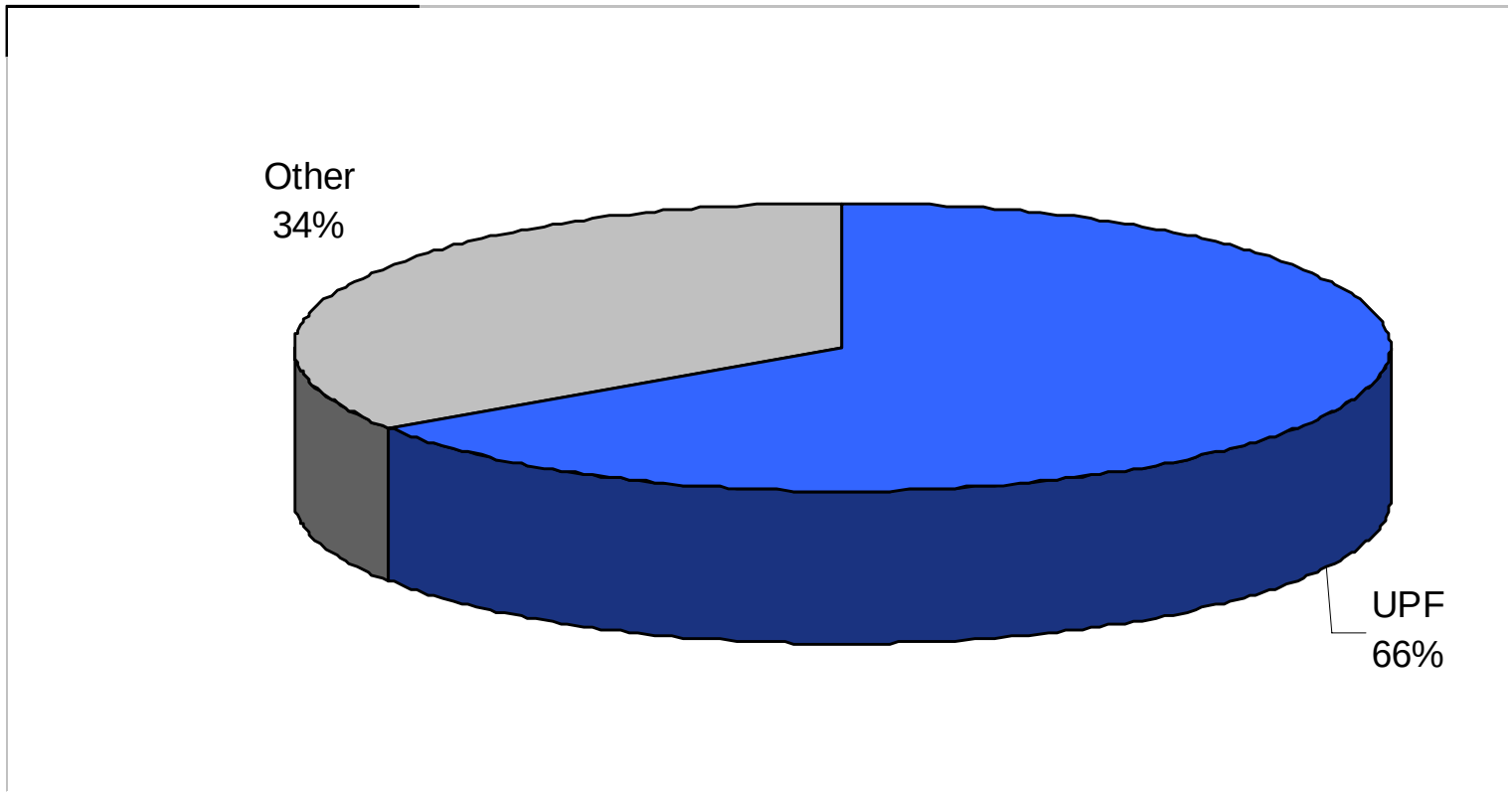
UPF EDA Support – Digital Design

COT/ASIC/FPGA Synthesis + Physical Implementation + DFT + Signoff



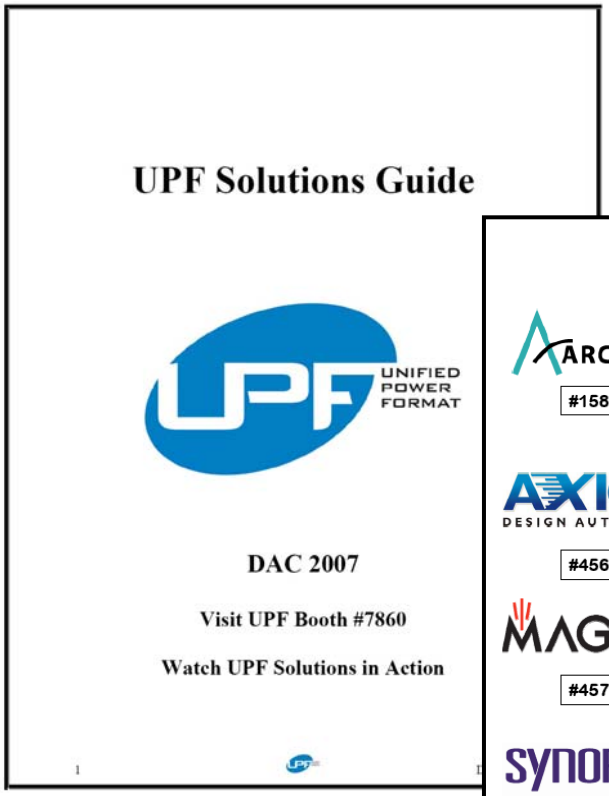
Based on Q4 05 through Q3 06 EDAC MSS data plus other publicly available market data

UPF EDA Support – Digital Simulation



Based on 2007 John Cooley DeepChip DevCon Survey "Mindshare" – 818 Respondents

Full Catalog of UPF Products



Company	Product	Usage
ArchPro	MaVeric	Verification
Atrenta	Spy Glass-Power	Analysis
Axiom	MPSim	Verification
Azuro	PowerCentric	Implementation
Magma	Talus Power	Implementation
Magma	Quartz Rail	Analysis
Mentor	Questa	Verification
Mentor	FormalPro	Verification
Springer	LP Methodology Manual	How-to Book
Synopsys	DesignWare IP	IP blocks
Synopsys	VCS	Verification
Synopsys	Design Compiler Ultra	Implementation
Synopsys	Power Compiler	Implementation
Synopsys	DFT Compiler/MAX	Implementation
Synopsys	Leda	Analysis
Synopsys	Formality	Verification
Synopsys	IC Compiler	Implementation
Synopsys	PrimeTime/PX,SI	Analysis
Synopsys	PrimeRail	Analysis
Synopsys	TetraMAX	Implementation
Virage	Silicon Aware IP	Low Power Libraries

Conclusion

- User community is actively guiding UPF
  - All leading users enthusiastically participate
  - Concepts are already production proven
- EDA community is strongly behind UPF
  - Supported by 9 out of 10 leading vendors
  - Interoperability is the key to success
- Next Step: IEEE standardization
  - World-wide adoption
  - Broad education effort needed