



Verification of Low Power Designs with VMM for Low Power

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ARM



The Architecture for the Digital World®

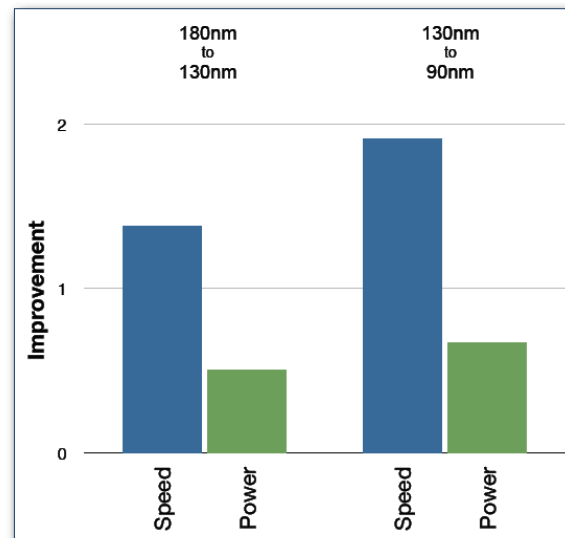


Low Power Design Trends

- **Users want more features in their mobile devices:**
 - MP3, Camera, Video, GPS...
- **But also need long battery life**
 - Convenient form factor, affordable price
- **Battery technology is not evolving fast enough!**
 - Need to manage power consumption

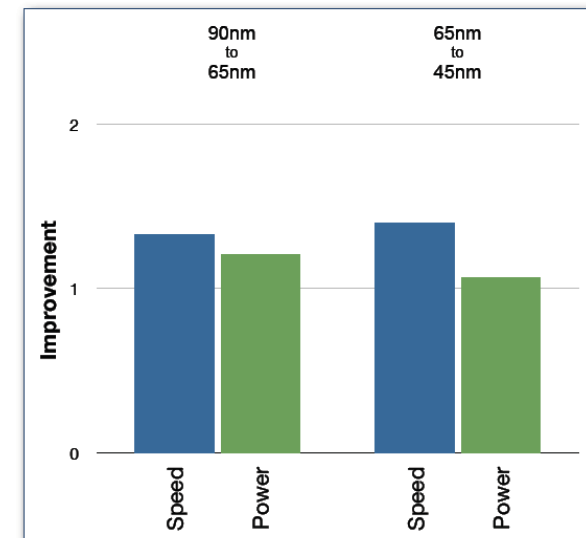


The good old days



Everything improves significantly

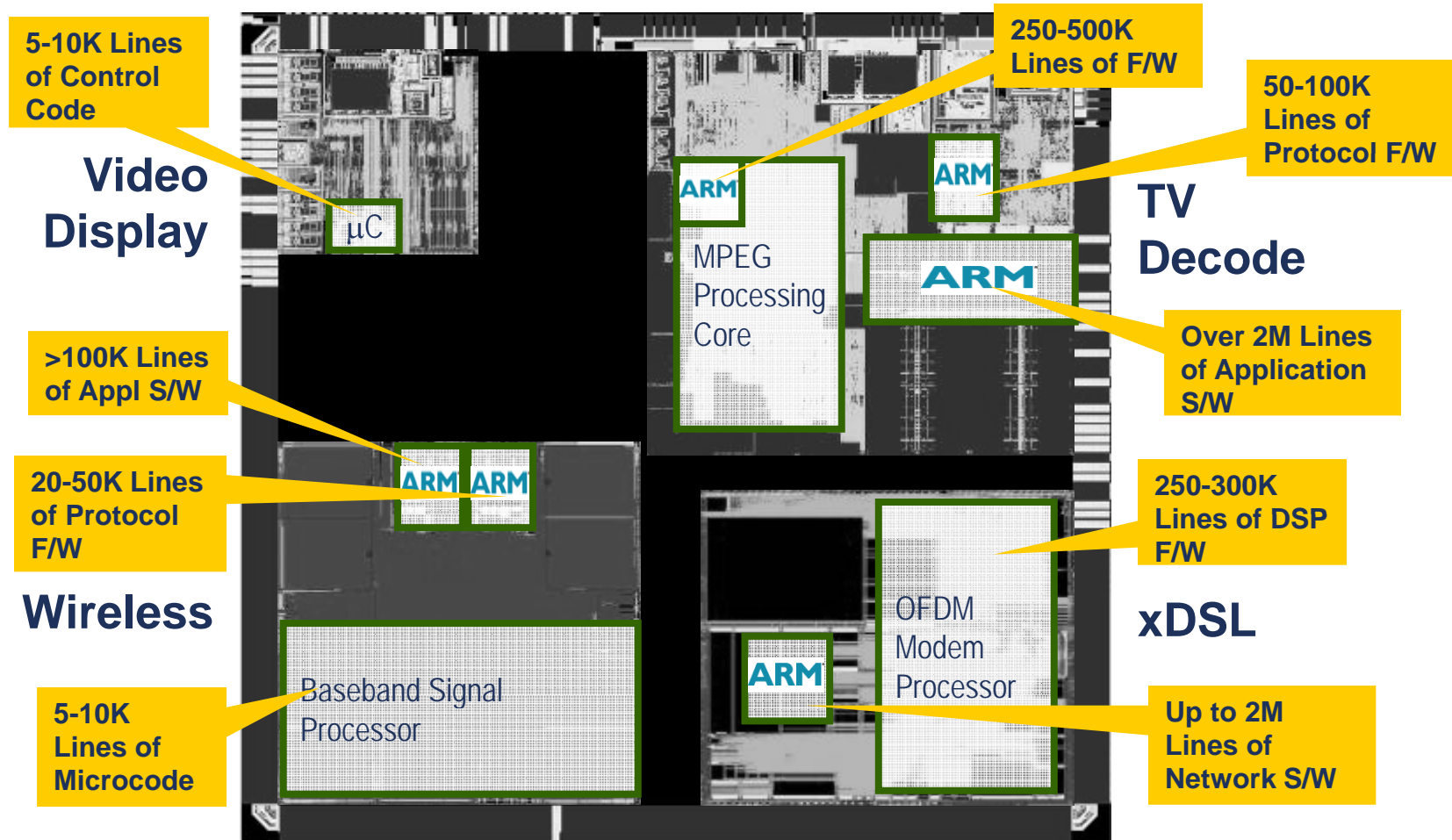
New reality



Speed increases at the expense of energy consumption



State Space Explosion



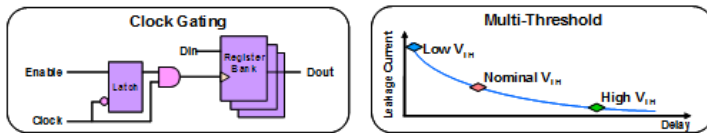
Nearly five million lines of code to enable Media gateway



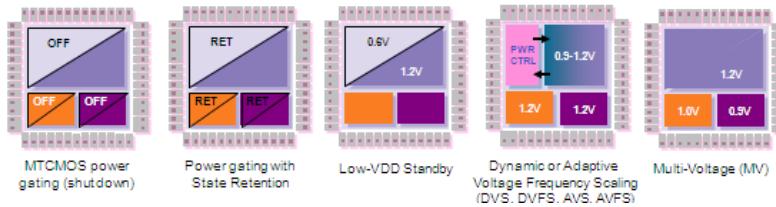
Low Power Design : Verification Impact

Range Of Low Power Design Techniques

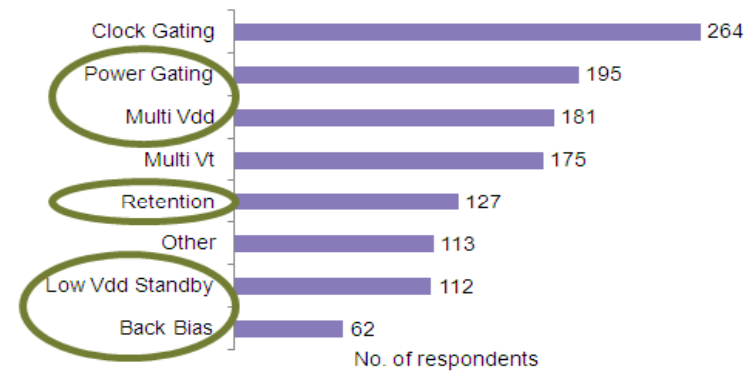
Traditional Techniques



Advanced Techniques

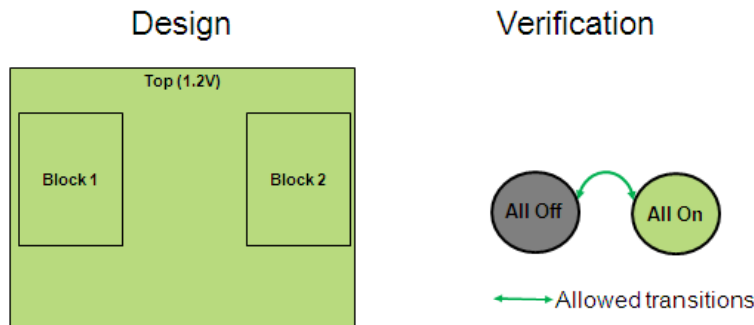


Over 50% Use Advanced Low Power Design Techniques

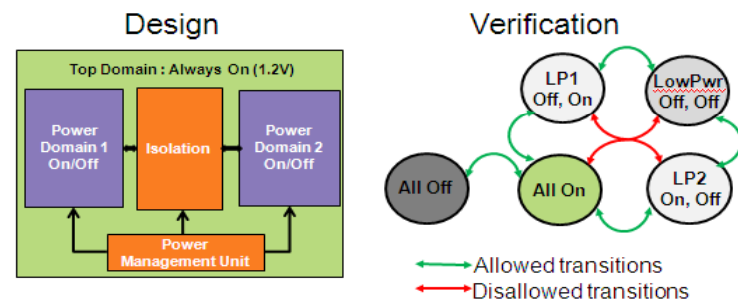


Which low power design techniques are you presently using?
2006 Synopsys Low Power Verification Webinar

Verification Of Non Low Power Designs



Verification Impact : Power Gating



Higher verification complexity vs. non low power designs

Need For Verification Methodology

- Low power verification tools don't enforce a verification methodology
- Ad-hoc verification may miss bugs
- Methodology must be comprehensive
- Leverage lessons learned to new projects

Methodology needs to be repeatable and scalable



Education

- Bugs related to low power techniques
- Documented examples from real designs
- Impact on Low power verification

Verification

- Low power perspective into verification planning
- Power -aware assertions and coverage

Reuse

- Power -aware base classes
- Best-practice rules and guidelines from over 30 companies

VMM for Low Power
Industry's First Low Power Verification Methodology

Strong Industry Alignment

“... The *Verification Methodology Manual for Low Power* is a timely and valuable resource that addresses all aspects of low power verification, providing detailed rules and guidelines.”



Jianfeng Liu
Senior Low Power Verification
Methodology Engineer

“... The VMM-LP provides clear insight into the pitfalls and practicality issues ... of low power systems. This handy volume comes with specific examples of design and verification issues that have been seen in actual chips...”

David Wheelock
SoC Power Architect, Seagate Technology

“... The *Verification Methodology Manual for Low Power* is a comprehensive collection of necessary and reliable techniques ... simplify and accelerate the complex task of verifying power-managed designs.”



Ying-Chih Yang
Technical Director of Home Entertainment Products

“Low power verification is the key challenge in low power design. The VMM-LP helps create a reusable verification environment for low power ... It helps find low power bugs and finds them early in the design cycle ... – savings in terms of mask costs and engineering debug time can be huge.”



K3 LP Group

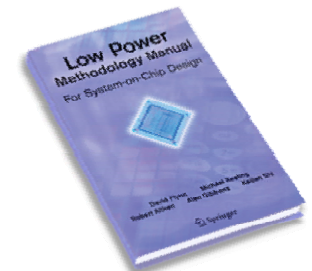
“We see a prevalence of low power designs in Japan ... VMM-LP is the answer to this market need and completely and elegantly addresses all aspects of low power verification...”

Nobuyuki Nishiguchi
VP and GM, Development Dept. 1



In Conclusion:

- **Power management is a system problem**
 - Impacts specification, architecture, implementation and verification
- **Need to ease adoption of advanced low power techniques**
 - Develop low power IP, tools & methodologies (IEM, PMK, LPMM, VMM-LP)
 - Low power verification is now a critical system verification activity
- **VMM for Low Power**
 - Provides methodologies, best practices, standardization and libraries for LP verification
 - ARM support VMM-LP as an important design-enabler for ARM processor-based system designs



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