

Design Flow Deployment

At-A-Glance

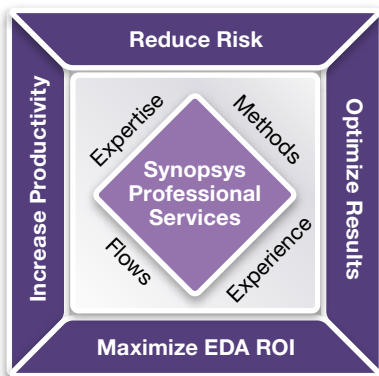
- ▶ Leverage expertise and design flows that are tapeout-proven at the most advanced process nodes
- ▶ Develop and optimize flows with the latest technologies and design techniques
- ▶ Customize/configure your Lynx Design System deployment

Optimize Your Design Flow To Address The Latest Design Challenges

Today's nanometer design geometries put tremendous pressure on design teams to maintain advanced design flows to achieve any satisfactory level of predictability and productivity in the chip design process. Timing closure remains the key design challenge, but power management issues are now on par with timing, and they are further complicated with the inter-related effects of signal integrity, manufacturability and testability. Design flows that were stretched to their limits to produce 130 or even 90 nanometer designs may not work at all at 65 or 40 nanometers without major enhancements.

Extensive experience with advanced designs, expertise with Synopsys' Galaxy™ and Discovery™ platforms, and significant investment in building and maintaining leading-edge flows in our own design centers make Synopsys Professional Services uniquely capable of helping you optimize your design flow for the challenges of implementing and verifying even the most advanced ASICs.

Because we're Synopsys, we're continually monitoring new tool releases and applying their most advanced features to our leading customers' design flows. And since Synopsys co-developed the reference flows for many of the leading IP providers and foundries such as ARM, TSMC, IBM, Global Foundries, UMC, SMIC and Common Platform, we are the natural choice to customize and deploy them into your production design environment.



Now, with the availability of the [Synopsys' Lynx Design System](#), you can deploy a complete, tapeout-proven RTL-to-GDSII flow that helps you address both design- and project-related bottlenecks. Our consultants are experienced users of Lynx, and can help you accelerate its deployment or customize it as necessary to meet your unique design environment requirements.

Analog/mixed-signal (AMS) IC designs face unique implementation and verification challenges at deep sub-micron processes. Modeling accuracy and silicon prediction behavior is more difficult, and growing design complexities and process effects increase memory capacity requirements and simulation run times beyond the efficiency of traditional post-layout flows. Synopsys consultants help you address common post-layout challenges by integrating Synopsys' Galaxy™ Implementation and Discovery™ Verification Platform features into your AMS verification flow.

The resulting, reusable flow improves the modeling and simulation accuracy of your designs while reducing run-times and memory requirements.

Whether you're at the beginning or in the middle of your design project, whether you need a minor upgrade to your flow or a complete production-ready design system to migrate to a new nanometer design node, Synopsys Professional Services will help you eliminate the bottlenecks that impact your design productivity.

Synopsys' Design Flow Deployment services include assistance with:

- ▶ Assessing of your existing design flow and environment
- ▶ Implementing of production-ready sub-flows for project-specific challenges (e.g., timing, SI, low power, design-for-test)
- ▶ Deploying of complete design flows to ease ASIC-to-COT or new technology node (e.g., 90nm, 65nm, 45/40nm, 32nm, 28nm) migrations
- ▶ Instantiating of customer-specific implementation methodologies (e.g., hierarchical or "virtual flat" design)
- ▶ Incorporating of new verification methods (such as assertions, functional coverage, and testbench automation) into existing environment
- ▶ Deploying and customization of the Lynx Design System (Production Flow and/or Foundry-Ready System) for customer-specific design environments, methodologies and process nodes
- ▶ Deploying of a reusable post-layout AMS flow with higher performance and better correlation to silicon
- ▶ Optimizing of extraction and simulation processes to improve simulation run time and memory capacity requirements
- ▶ Validating of new a new flow or sub-flow with a "pipe-cleaner" design and/or test chip

To get more information on how we can customize our services to help you meet your design goals, please [contact us](#) or call your local [Synopsys sales representative](#).



Predictable Success Synopsys, Inc. • 700 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

©2010 Synopsys, Inc. All rights reserved. Synopsys is a trademark of Synopsys, Inc. in the United States and other countries. A list of Synopsys trademarks is available at <http://www.synopsys.com/copyright.html>. All other names mentioned herein are trademarks or registered trademarks of their respective owners. 05/10.CE.10-18574.