

De-risking Variation-Aware Custom IC Design with Solido Variation Designer and Synopsys HSPICE

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Authors Introduction

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Challenges in a traditional custom IC variation-aware design flow lead to schedule, product yield, and product quality risks. Solido Variation Designer and Synopsys HSPICE® together enable fast and accurate variation-aware design methods that can reduce or remove risks associated with traditional variation-aware design. Together, these tools and methods help to reliably deliver products on schedule that are competitive and cost-effective.

Variation-Aware Design Risks

Variation is affecting custom IC designs increasingly as process technologies shrink, and designing for variation is now a required step in successfully delivering a product. To enable design for variation, foundries release models that describe the variation. These models can provide excellent insight as to how variation will affect a design. The design challenge is to make the most effective use of the foundry models to measure the effects of variation, to optimize the design for variation, and to do so within the tight product design schedule. Ineffective variation-aware design adds schedule risk, product yield risk, and product quality risk.

Schedule risk: Designing for variation has traditionally required considerable time and effort, while providing limited guidance to the designer on how to improve the design. Methods like simulating process corners and running Monte Carlo analysis require hundreds or thousands of SPICE simulations. The main schedule risk comes from these analyses being run as a verification step, and problems found lead to unplanned design iterations. Furthermore, the information produced by these analyses provides limited guidance to the designer, which means that fixing variation problems can require several iterations of trial-and-error, with an expensive verification process repeated each time. This schedule risk occurs both during the pre-layout and post-layout design phases.

Product yield risk: Given limited schedule time to address variation, often variation-aware design steps are cut short and are not particularly accurate. For example, only a handful of process corners may be run, and failure cases may be missed, Monte Carlo analysis may be limited to too few simulations to accurately verify the design, and variation-aware checks may be skipped post-layout and can miss parasitic and proximity induced variation problems. These shortcuts can lead to reduced product yield and respins.

Product quality risk: When variation problems are found in the design, the step of fixing them can take considerable time. Without useful guidance and limited schedule time, the designer must fix the variation problems quickly using ad-hoc analyses and rules of thumb. Typically, device geometries are increased to make them more resilient to mismatch effects, and current is increased. Often, due to imperfect information about the effects of variation on the design, these steps are done imprecisely, wasting area, performance, and power, and ultimately making the designs less competitive.

Solido Design Automation and Synopsys have partnered to provide a comprehensive, fast, and accurate variation-aware custom IC design solution. Together, they reduce variation-aware design risks to reliably deliver competitive, profitable products on schedule. This paper discusses methods for eliminating schedule, product yield, and product quality risks that are enabled using Solido Variation Designer and Synopsys HSPICE.

Seamless Integration

Variation Designer and HSPICE are seamlessly integrated, making them convenient and efficient to use together for addressing variation.

Variation Designer automatically drives variation-aware experiments using HSPICE. Variation Designer parses variation information from the HSPICE model files directly, and then inserts experimental variation settings into the netlist automatically. As an even more reliable and efficient mechanism, Variation Designer can also read the HSPICE Variation Block, and can drive variation-aware designed experiments using HSPICE External Sampling.

HSPICE's waveform post-processing delivers results quickly and reliably with reduced I/O and without third party tools or additional licenses. Variation Designer reads the HSPICE results directly. Variation Designer then helps the designer to interpret the raw results using useful visualizations, and can open waveforms using popular waveform viewers used with HSPICE.

This comprehensive integration ensures that Variation Designer and HSPICE work reliably together in the design flow, enabling low-risk variation-aware design with little integration or support overhead.

Reducing Schedule Risk

Variation-aware design can be time-consuming, and can lead to unpredictable schedule overruns. Some common sources of schedule problems include failures in long-running analyses requiring the analyses to be repeated, poorer than expected simulation throughput, and unplanned iterations for fixing variation problems. Using Variation Designer with HSPICE, these risks can be avoided so that designs are delivered on schedule.

Completing PVT and Monte Carlo analyses reliably

PVT and Monte Carlo analyses can take several tries to set up and run successfully to completion, which puts schedules at risk. These types of analyses have long runtimes, but often are plagued with problems and need to be run multiple times for the analysis to complete without crashing or simulation failures occurring along the way. When parallelizing simulations, the chance of failure increases due to unstable compute nodes, parallelization errors, and increased network dependencies. These kinds of errors can require re-running an already long job multiple times, which can unexpectedly add days to a schedule.

Variation Designer and HSPICE together form a resilient simulation engine, which can eliminate unexpected delays in completing variation-aware analyses. Reliability starts at the simulator, and HSPICE provides excellent debugging messages in its simulation log files. HSPICE also post-processes its waveforms using a reliable, built-in metrics definition language rather than relying on a third party tool for this function, making it faster and more reliable for post-processing.

Variation Designer wraps HSPICE's reliability with a resilient simulation environment. It begins with a streamlined setup, which enables fast experimental design and catches setup errors before starting the simulation job, so that the job is configured correctly the first time. When errors occur at runtime due to simulations not converging, problems on the cluster, network problems, disk errors, etc., Variation Designer clearly highlights those failures. Moreover, Variation Designer enables the designer to inspect the error, to correct it using Variation Designer's powerful simulation debugging console, and to re-run the simulation that had errors, leading to error-free results without having to re-run the whole simulation job.

By using Variation Designer and HSPICE together, simulation jobs finish faster and correctly the first time. This eliminates the unexpected need to re-run long variation-aware analyses, reducing schedule risk.

Increasing PVT and Monte Carlo speed with a scalable parallel simulation engine

One way to speed up variation-aware design is to parallelize long running jobs across a multi-core machine or on a simulation cluster. However, the return from doing this can be non-linear, and diminishes as additional compute nodes are added, limiting the potential for speeding up variation-aware design, as shown in Figure 1.

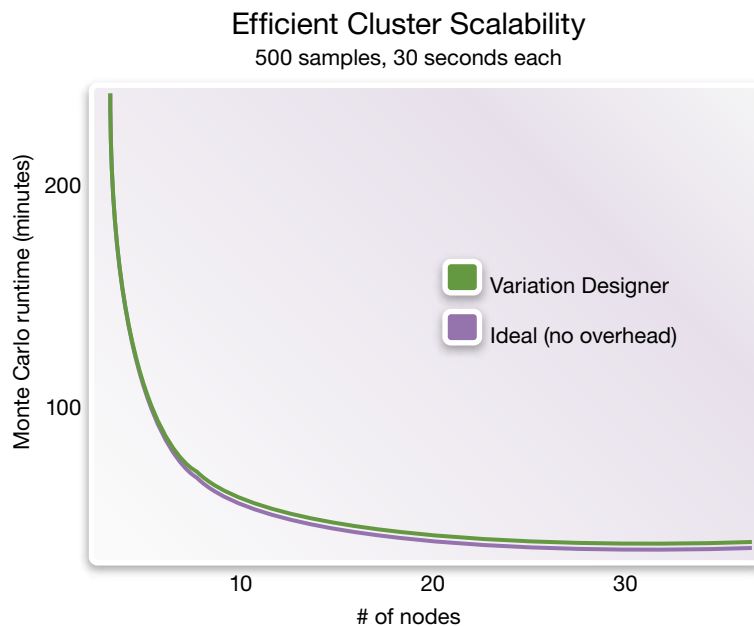


Figure 1: Variation Designer and HSPICE have near perfect throughput scaling when used on a cluster, even with fast-running simulations. The ideal line on this plot shows a hypothetical runtime with perfectly linear scaling with the number of computer nodes, which is very closely approached by Variation Designer and HSPICE.

Variation Designer's parallelization engine is designed for optimal performance, both running on multi-core computers, and for running on large clusters. The simulation engine has been developed, tested, and tuned over several years to remove common bottlenecks in parallelizing simulations, such as overhead from staging simulations, delays while checking out licenses, high peak disk I/O from simulations, and heterogeneous cluster performance. HSPICE's fast start-up time and simulation post-processing further help to optimize throughput on a cluster.

Using Variation Designer and HSPICE with a cluster, variation-aware design can be performed more quickly by scaling efficiently and ensuring outstanding cluster throughput. This eases schedule constraints, and enables catch-up on projects that are running behind schedule by increasing the simulation cluster size.

Designing for variation from the start

Detecting and fixing variation problems sooner in a design leads to more predictable schedule outcomes with fewer surprises and faster delivery. Yet, variation analysis is often reserved as a verification step, after considerable effort may have already been invested in tuning the design. The product may appear to be on schedule at this point, but variation problems found later can lead to major design changes, discarding previous tuning work, and setting the schedule back.

Using HSPICE with Variation Designer enables designers to gain insight into the effects of variation earlier in the design cycle by extracting and designing to variation corners, and by leveraging variation-aware sensitivities and sweeps.

Extracting PVT corners: Finding extreme PVT corner cases to design against is easy and fast using Variation Designer's design of experiments options. In just 10s of simulations, it is possible to explore the whole PVT space and, using Variation Designer's PVT corner prediction, to find likely worst case corners for each output. These PVT corners are excellent estimators of variation effects, and are useful to design to.

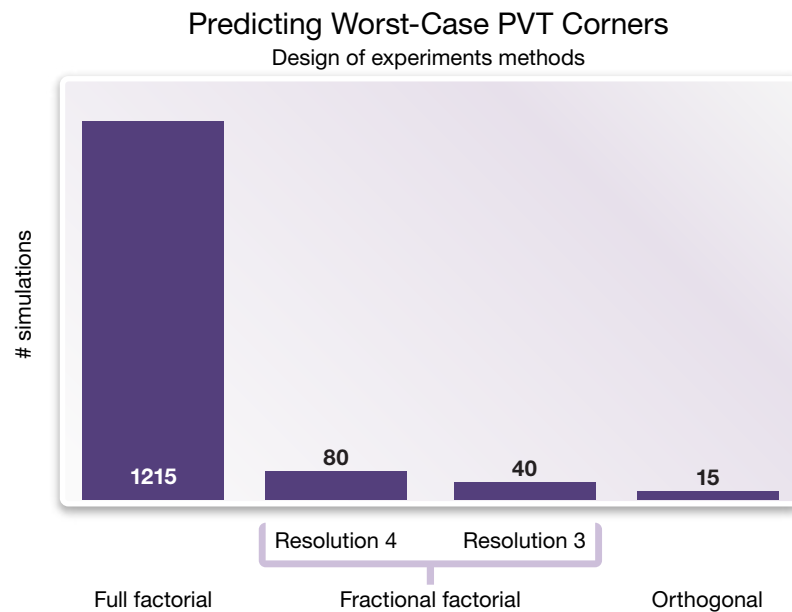


Figure 2: Variation Designer can predict worst-case PVT corners in just 10s of samples with its design of experiments (DoE) options. This example shows the number of simulations required to explore a PVT space with 5 process corners (FF, SS, etc.) and 5 other variables (temperature, voltage, etc.) with 3 values each. The orthogonal DoE is the fastest, but does not consider interactions among variables, while the fractional factorial methods include interactions efficiently by designing perfectly balanced experiments that enable accurate results through regression.

Extracting statistical corners: Variation Designer's statistical corner extraction feature can find statistical outliers at the target sigma in just 10s or 100s of simulations. It works by running a sufficient number of Monte Carlo samples to estimate the distribution using density estimation, finds the location in the distribution that represents the target sigma, then finds corners at the target sigma with adaptive learning and tuning. This produces corners that represent the target sigma in the output distribution, which are ideal estimators of statistical variation effects to design to.

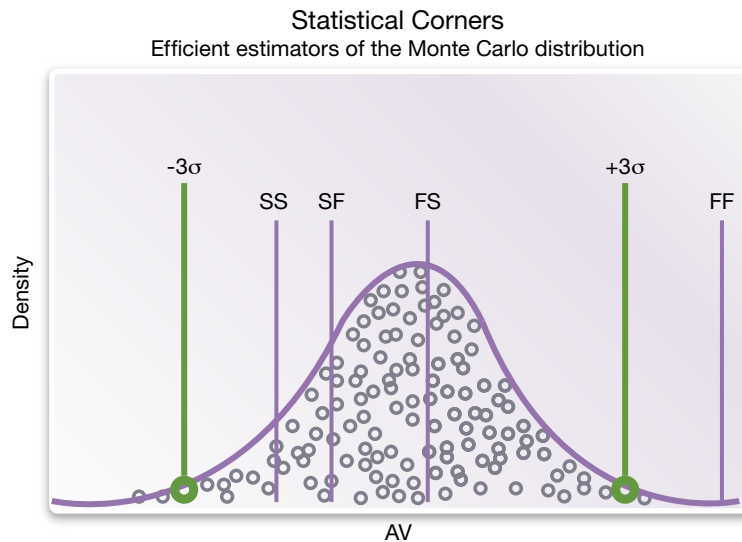


Figure 3: Variation Designer can extract corners at a target sigma in just 10s or 100s of simulations.

Designing to corners: Once variation-aware corners are extracted, the designer can quickly design to these corners instead of to nominal. This gives insight throughout the design phase. Variation Designer’s Run Extracted Corners app is designed specifically for this, enabling predicted worst-case PVT corners and statistical corners to be re-run with a single click. Simulation results are displayed such that it is easy to compare changes to variation bounds with design iterations, enabling rapid design tuning and variation analysis iterations, similar to how iterations at nominal are traditionally done.

By using HSPICE with Variation Designer to detect variation problems sooner and to design for them from the first design iteration, verification succeeds more reliably, and there are fewer surprise design iterations.

Avoiding proximity problems

Proximity effects introduced during layout cause systematic shifts in performances. These shifts can be detected in post-layout simulations. However, pinpointing the causes of proximity problems and fixing them is a tedious task that typically requires considerable trial and error and several iterations with layout. When proximity problems are introduced, they can unexpectedly set back design schedules by days or even weeks.

Variation Designer can determine minimum safe well proximity settings prior to layout, which eliminates well proximity problems entirely, along with the tedious and time-consuming work to detect causes and fix problems.

By designing for variation using reliable, fast, and accurate tools that enable variation-aware design earlier in the design cycle, time spent designing for variation can be planned for, and schedule risk from variation is nearly eliminated.

Reducing Product Yield Risk

Product yield problems can be caused by failing to run the true worst-case PVT corners, skipping Monte Carlo analysis, running Monte Carlo with too few samples, or skipping post-layout variation-aware analyses. These shortcuts are often taken because of schedule pressures which prevent thorough verification. Long simulation times, unreliable tools, and poor insight from simulation investment contribute to trimming variation verification steps when under schedule pressure, leading to higher fabrication costs, and sometimes expensive respins.

A variation-aware design flow using Variation Designer and HSPICE virtually eliminates yield risks due to variation. Together, they can increase the PVT corner coverage, deliver higher Monte Carlo accuracy, and enable more rigorous post-layout variation analysis, all within the schedule constraints of a production environment.

Increasing PVT corner coverage

Simulating all possible combinations of process corners, voltages, temperatures, loads, and other variables is usually infeasible within a production schedule. Instead, designers typically select a small subset of PVT corners that are likely to cause failures, and limit PVT analysis to only those corners. This adds risk of missing worst case corners, leading to unforeseen yield loss or respins. This problem is even more significant at smaller process nodes, where variation behaves in less conventional ways, making it less reliable to guess at worst cases.

Setting up PVT corner combinations can be tedious and error prone. Variation Designer enables the designer to set up advanced combinations of PVT corners in under a minute. This reliable and fast setup enables more time to be spent running simulations and evaluating results, and less time setting up experiments.

Using Variation Designer with HSPICE to run corners, more corners can be run in less time than with conventional PVT corner tools. This enables more thorough coverage for PVT combinations with the same level of investment in simulation time.

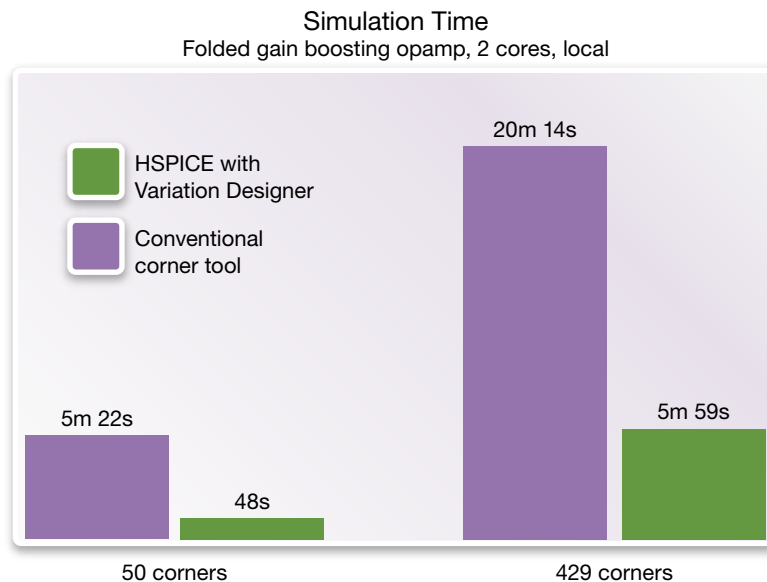


Figure 4: Variation Designer's efficient simulation engine combined with HSPICE's fast simulation time run more corners in less time than conventional corner tools. This example shows large speed-ups in total wall clock time when running 50 and 429 corners on a gain-boosting op amp design, running the simulations. using two cores on the local machine.

Rather than guessing which corners are the worst based on previous experience, designers can also use Variation Designer's worst case corner prediction features to find more likely worst cases by efficiently exploring the whole PVT space, building a sensitivity model, and using the model to predict worst case corners. This feature can leverage a suite of design of experiments methods to deliver the best corner prediction accuracy possible within the available simulation budget.

Whether running a custom set of PVT corners or using worst case corner prediction, Variation Designer automatically post-processes all simulation data and displays it using helpful visualizations. The effects of variation on each output are immediately clear, sensitivities are clearly shown, and scatterplots clearly show tradeoffs between outputs. These powerful visualizations were custom tailored using the input from dozens of production designers to eliminate the need to manually post-process information, as well as to reveal more from every PVT analysis.

Keeping the history of changes in the session, regardless of activity, allows designers to explore avenues, roll back changes, modify their approach and benefit from the system's long and accurate memory.

PVT Visualization



Figure 5: Variation Designer's PVT visualizations help to see the effects of variation clearly without the need to post-process data manually or to generate plots with third party tools.

Improving Monte Carlo accuracy

Monte Carlo analysis takes a long time to run to accurately verify product yield. For example, to verify a design to 3-sigma requires over 1500 samples to verify that yield exceeds the 3-sigma target using a binomial confidence interval with 95% statistical confidence. For each sample, the analysis needs to be run across all temperature, voltage, etc. conditions, and to be run for each separate testbench, resulting in thousands of simulations to conclusively verify a design to 3 sigma. Production schedules often do not permit this thorough analysis, so Monte Carlo is limited to a smaller number of samples. Though this limited analysis can provide an approximation of yield, it may be inaccurate and can lead to unanticipated yield problems in production. When schedules are particularly tight, Monte Carlo analysis is sometimes skipped entirely, which can lead to poor yield and respins due to mismatch variation or other design-specific conditions which can only be revealed using statistical methods.

Variation Designer and HSPICE together make it possible to run a more thorough Monte Carlo analysis within the constraints of a production environment. This tool combination enables several ways of improving Monte Carlo runtimes and delivering greater accuracy in less time. Variation Designer's accuracy-aware visualizations also provide feedback to know when a design is adequately verified to prove or disprove product yield goals, avoiding wasted simulations and uncertainty about how many simulations to run.

Being able to drive more samples in less time is an easy way to increase accuracy. Variation Designer's high performance control engine scales efficiently to drive more simulations in less time (see Figure 1), and can drive Monte Carlo simulations quickly, even for large designs (see Figure 6).

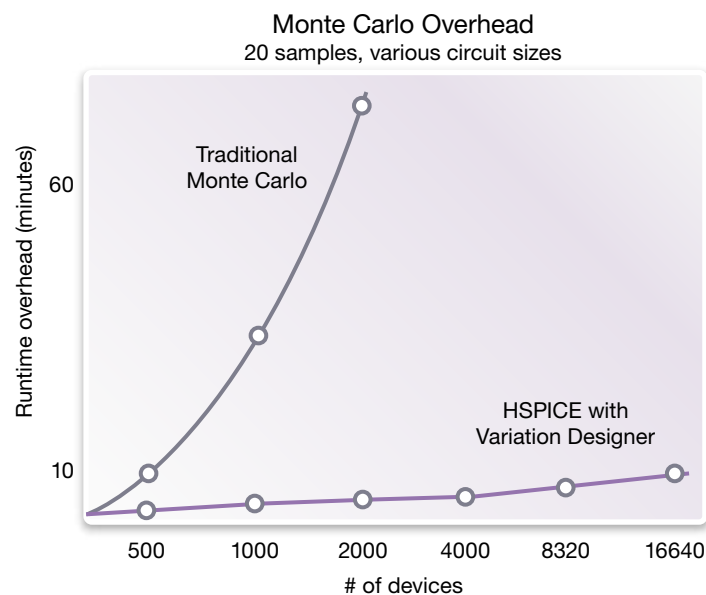


Figure 6: Variation Designer's High capacity Monte Carlo drives more samples in less time for larger circuits than conventional Monte Carlo engines. This plot shows how Monte Carlo runtime, excluding simulation time, is nearly linear using Variation Designer, while traditional Monte Carlo tools have exponential Monte Carlo overhead.

Variation Designer's Optimal Spread Sampling better selects samples to achieve up to 10x better accuracy with the same number of samples as traditional random Monte Carlo, and provides on average 1.6x more accurate results than Latin Hypercube sampling.

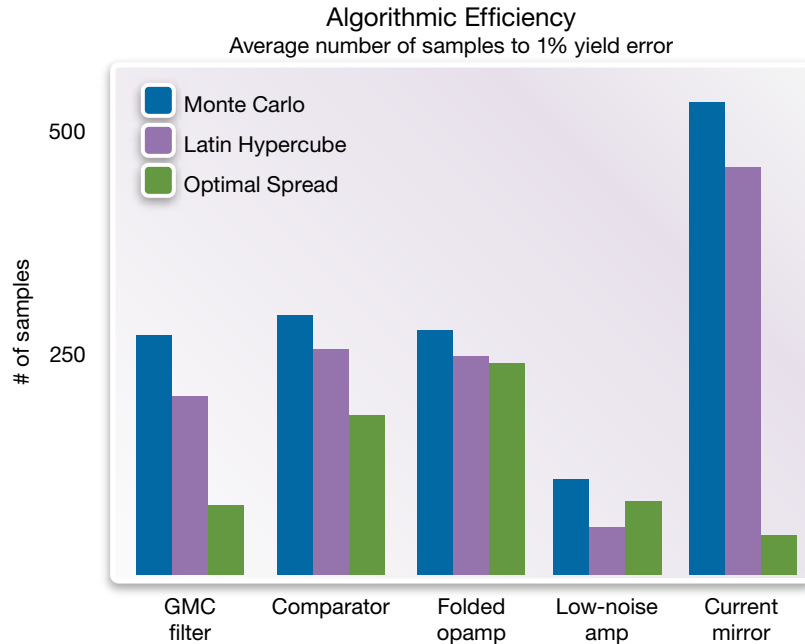


Figure 7: Variation Designer's Optimal Spread Sampling delivers better yield accuracy in fewer samples than traditional Monte Carlo methods.

Variation Designer automatically calculates the accuracy of Monte Carlo analysis in a variety of ways, so it is always clear how accurate the yield estimate is. Some features included for estimating yield accuracy include (See Figure 8):

- ▶ The minimum and maximum yield are shown based on the number of samples run, using a 95% binomial confidence interval
- ▶ A yield accuracy plot shows yield accuracy convergence with the number of samples
- ▶ The mean and standard deviation convergence plots show how these important statistical measures are converging with number of samples
- ▶ A density estimate shows the predicted shape of the distribution and calculates partial yield and yield estimates using the density curve
- ▶ Accuracy of impacts is calculated using bootstrapping, revealing the accuracy of causes of variation problems

Accuracy-Aware Monte Carlo

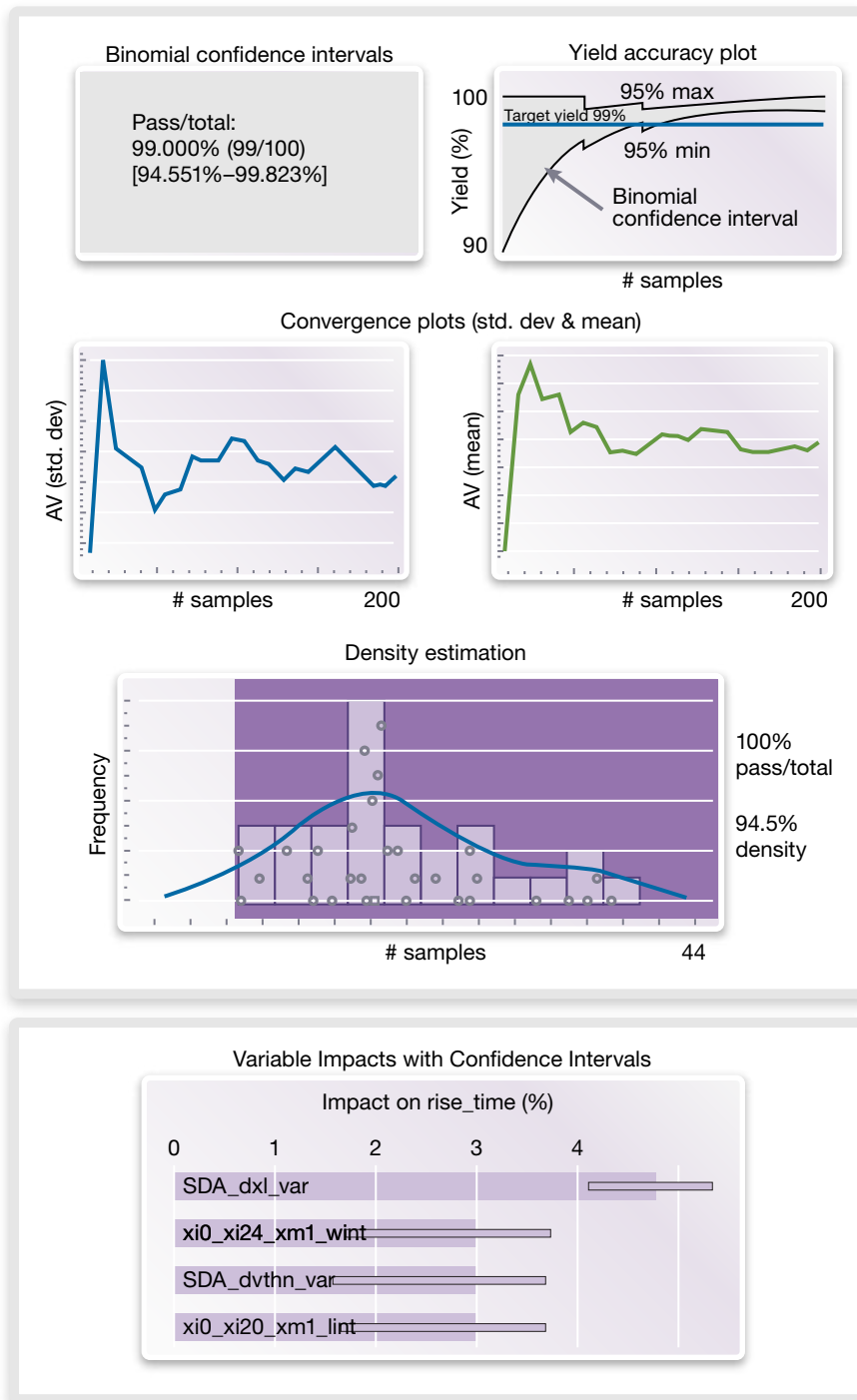


Figure 8: Variation Designer’s accuracy-aware Monte Carlo includes a suite of features that reveal precisely how accurate yield estimates are to the designer.

Selecting the correct number of samples to run in order to achieve a desired level of accuracy is automated with Variation Designer. This is done by entering the target sigma or yield, then dynamically, at runtime, stopping when the target yield crosses the bounds of the binomial confidence interval. This is impossible to calculate ahead of time, as the binomial confidence interval depends on the number of observed failures and passes.

Monte Carlo Verification Running the correct number of samples

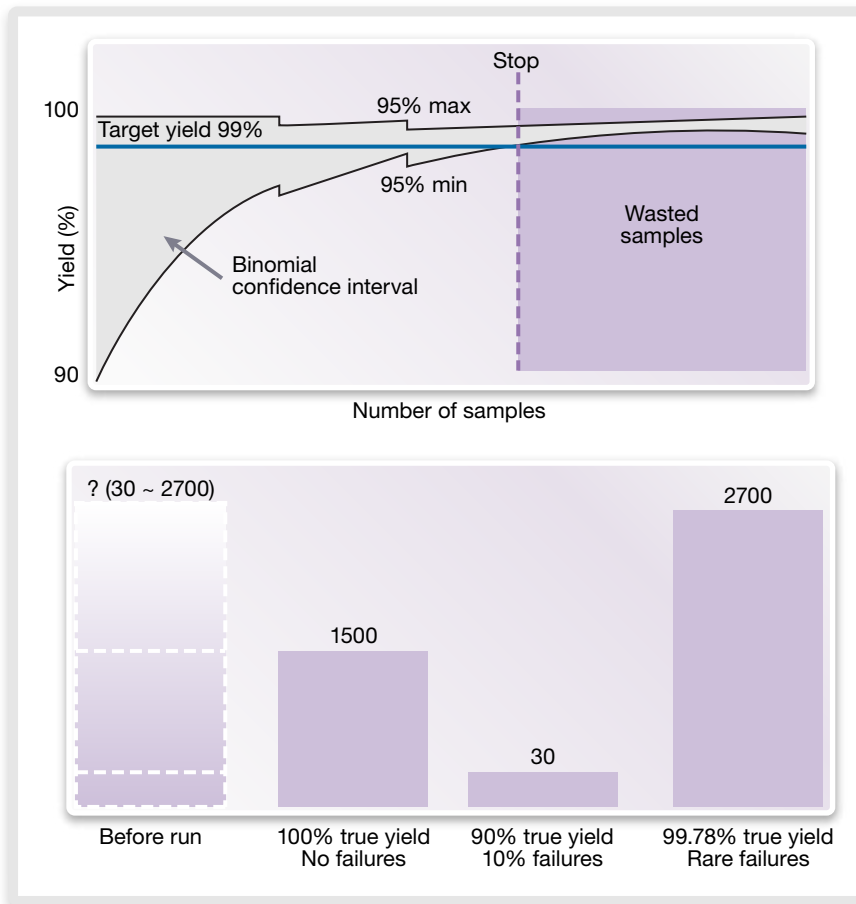


Figure 9: Variation Designer always runs the correct number of samples to verify the design to the target sigma by stopping when the target yield leaves the binomial confidence interval. The correct number of samples varies based on the true yield of the design, which is determined at runtime and cannot be calculated ahead of time. This saves simulations by running the minimum number of samples to prove or disprove the desired yield accuracy.

Verifying post-layout with PVT corners and Monte Carlo

Post-layout verification simulation times are typically much longer than pre-layout runtimes due to parasitics in the netlist. For this reason, post-layout verification using simulation is limited, typically only a small number of PVT corners are run, and Monte Carlo is skipped.

By using Variation Designer to find the worst-case PVT corners in pre-layout, post-layout simulations can be more effectively focused on the true worst-cases from pre-layout. This makes the most out of a limited simulation budget. If layout effects are suspected to have changed the worst-case PVT corners from pre-layout, Variation Designer's efficient design of experiments and parallelization can be used to efficiently explore the PVT space and find potential changes while keeping the number of simulations to a minimum (see Figure 2).

Due to long simulation times, thorough Monte Carlo analysis is typically not practical, but this does not preclude the use of Monte Carlo for an acceptable statistical smoke test. Using Variation Designer's efficient scalability to handle the larger number of devices post-layout (see Figure 6), combined with the improved accuracy of Optimal Spread Sampling (see Figure 7) and effective cluster distribution (see Figure 1), post-layout Monte Carlo can be run with a smaller number of samples and the distribution checked against pre-layout results to ensure that there are no major differences due to layout effects.

More thorough coverage of the PVT space, faster and more accurate Monte Carlo analysis, and more rigorous post-layout variation analysis contribute to reducing product yield risks. This, in turn, reduces product cost, and can avoid costly respins.

Reducing Product Quality Risk

Schedule pressures and imprecise variation-aware design guidance often leave the designer little choice for fixing variation problems. Rather than precisely identifying the cause of the problem and fixing it efficiently, they are forced to resort to rules of thumb, scaling up suspect devices, pumping more current through devices, or trading off other performances to boost outputs affected by variation. Additionally, because the designer does not typically know if they have truly found the worst case PVT corners or if their Monte Carlo analysis is sufficiently accurate, they may leave additional design margin to compensate for the uncertainty, to help ensure that product yield goals are met. This results in lower quality designs that use more power and do not perform as well, and that are more expensive to manufacture due to larger design area.

Variation Designer helps to eliminate the need to over-design by accurately analyzing the PVT, statistical, and proximity spaces, by identifying the precise causes of variation problems, and by revealing variation-aware improvements to device geometries.

Tightening design margins with improved variation-aware precision

Tightening design margins requires more accurate information about how variation will affect the design. This added insight can be obtained using methods described above, including designing for variation earlier in the design cycle, increasing the thoroughness of PVT verification, using accuracy-aware Monte Carlo and proximity analysis, and by designing to worst case PVT corners and statistical corners at the target sigma.

Identifying precise causes of variation problems

Finding causes of variation problems can be a time-consuming, ad-hoc process, requiring many simulations to complete, and often producing results that are too imprecise to lead to effective design improvements. For example, designers may add voltage sources to their schematic to emulate a voltage offset mismatch condition. While these kinds of experiments can provide some insight into the robustness of the design, they are not representative of what is modeled by the foundry, and can even be misleading to the designer.

To simplify the process of assessing causality of variation problems, Variation Designer provides sensitivities and impacts with both PVT and Monte Carlo analyses, which can reveal the precise causes of variation problems with no additional simulations or experiments. This information can often be sufficient to guide the designer to effectively solve the design problem without over-designing.

Impacts and Sensitivities



Figure 10: Variation Designer provides PVT sensitivities and Monte Carlo impacts, revealing causes of variation problems with no additional simulations.

Running variation-aware geometry sweeps

It is common to analyze the effects of changing geometries by sweeping values of lengths and widths. When sweeps are performed over nominal conditions, they can show how the nominal performance may shift up or down with changes to the geometries. This ignores variation effects, which cause output distributions to also expand and contract with changes to geometries.

Using extracted PVT and statistical corners, Variation Designer can add variation-awareness to geometry sweeps, revealing the effects of variation on geometry changes. This better enables the designer to accurately identify the best geometries to use for improving performances while considering the effects of variation. Similarly, variation-aware sensitivity analyses can find the devices that are the most effective to tune in order to reduce the effects of variation.

Reducing area and power

Area and power are commonly over-designed in order to account for undetected variation effects. Using accurate extracted PVT and statistical corners, design margins can be tightened without adding yield risk. However, finding area and power reduction opportunities can still be tedious if done through trial-and-error.

To quickly identify area reduction opportunities, Variation Designer's area reduction feature can be used to find devices that can be safely reduced in size without increasing variation effects on outputs.

To reduce power consumption, an output that measures the approximate power consumption of the circuit can be set up to enable Variation Designer to analyze power tradeoffs with variation effects on other outputs. Variation Designer's variation-aware sweeps and device sensitivity features can then be used to find ways of implementing power savings while keeping other performances within specification.

Area and power improvements can thus be implemented in the design, then quickly verified by running extracted PVT and statistical corners to ensure that the changes had the desired effects.

Reducing proximity guardband area

To avoid the well proximity effect, devices are often guardbanded using a 2- or 3-micron guardband. For most devices, these guardbands are unnecessary, as performances are unaffected using design rule minimum well distance values. For the remaining handful of devices, the standard 2-3 micron guardband is required, and in rare cases, the default guardband is insufficient. The challenge is that the designer does not know which devices require guardbanding, and so many devices are guardbanded unnecessarily.

Variation Designer's well proximity feature determines the minimum safe well spacing for each device prior to layout, which reduces guardband area by up to 90% and total design area by up to 30%.

By more precisely designing for variation, unnecessary design margins are eliminated, producing higher-performance, lower-power, and smaller-area designs that are more competitive and cheaper to manufacture.

Conclusion

Using Synopsys HSPICE with Solido Variation Designer reduces risks and provides a fast, accurate variation-aware custom IC design flow, leading to competitive products that are more economical to manufacture and delivered on time. To learn more about ways to reduce variation-aware design risks or to enquire about other variation-aware solutions, please contact Solido or Synopsys directly

