

Shorter Turnaround Time (TAT) With In-Design Physical Verification

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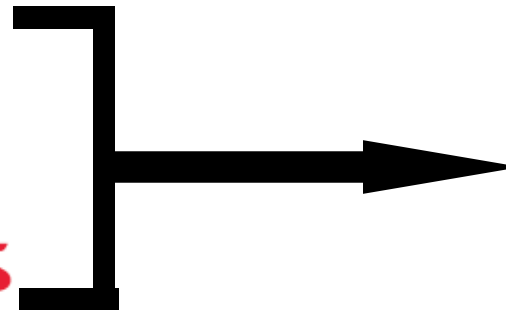
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Design Automation Conference

About Renesas Electronics

NEC
NEC ELECTRONICS

RENESAS

Renesas Technology Corp.



RENESAS

Renesas Electronics

The world's third largest semiconductor supplier

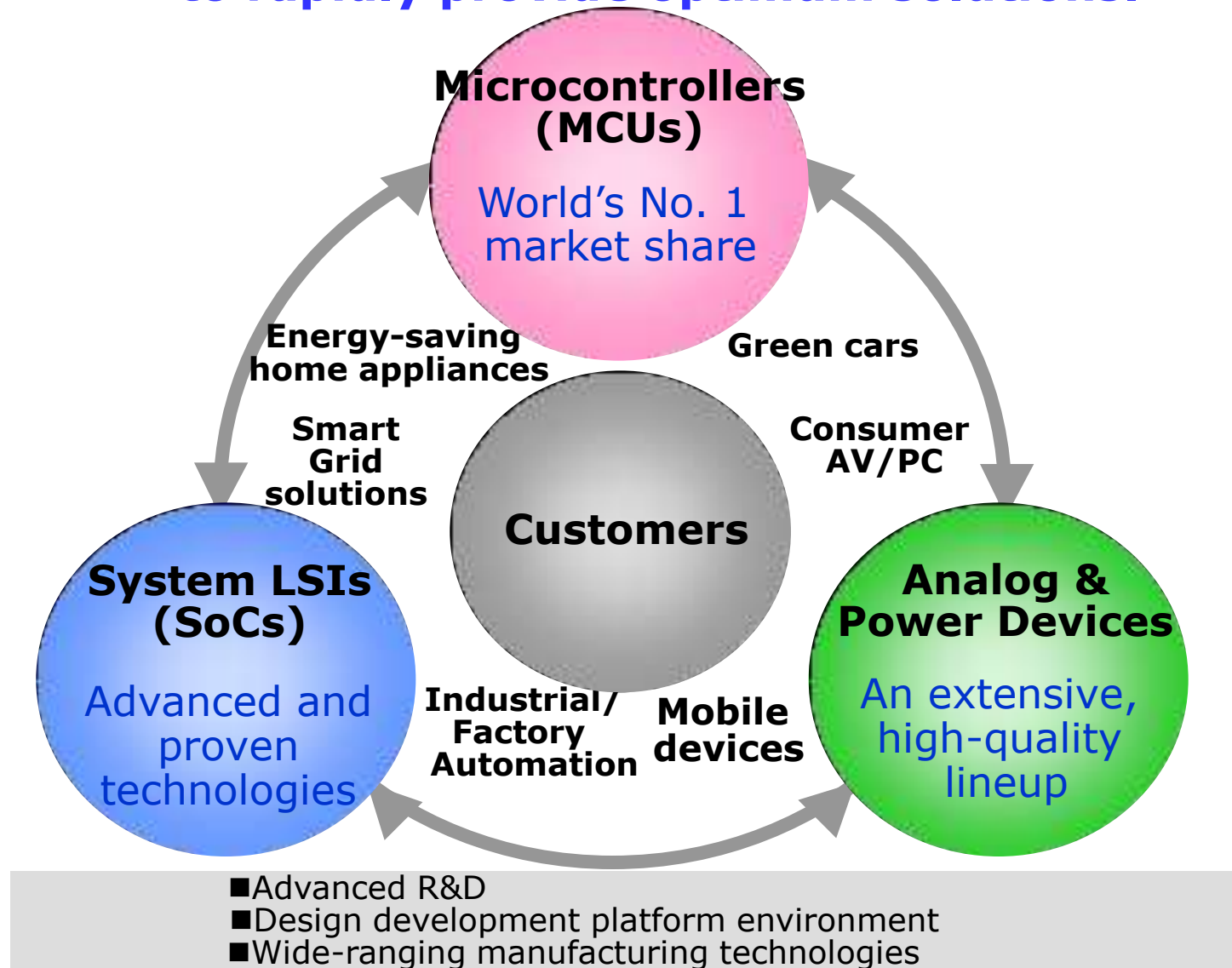
Worldwide Semiconductor Suppliers: CY2009 Revenue Ranking

2009 Rank	Supplier	2009 Revenue (\$M)	2009 Share
1	Intel	33,253	14.6%
2	Samsung Electronics	17,686	7.7%
3	Toshiba	9,604	4.2%
4	Texas Instruments	9,142	4.0%
5	STMicroelectronics	8,510	3.7%
6	Qualcomm	6,409	2.8%
7	Hynix Semiconductor	6,035	2.6%
8	Renesas Technology	5,670	2.5%
9	AMD	5,157	2.3%
10	Infineon Technologies	4,682	2.1%
11	NEC Electronics	4,542	2.0%
12	Broadcom	4,317	1.9%

Renesas Electronics Corporation
\$10,212

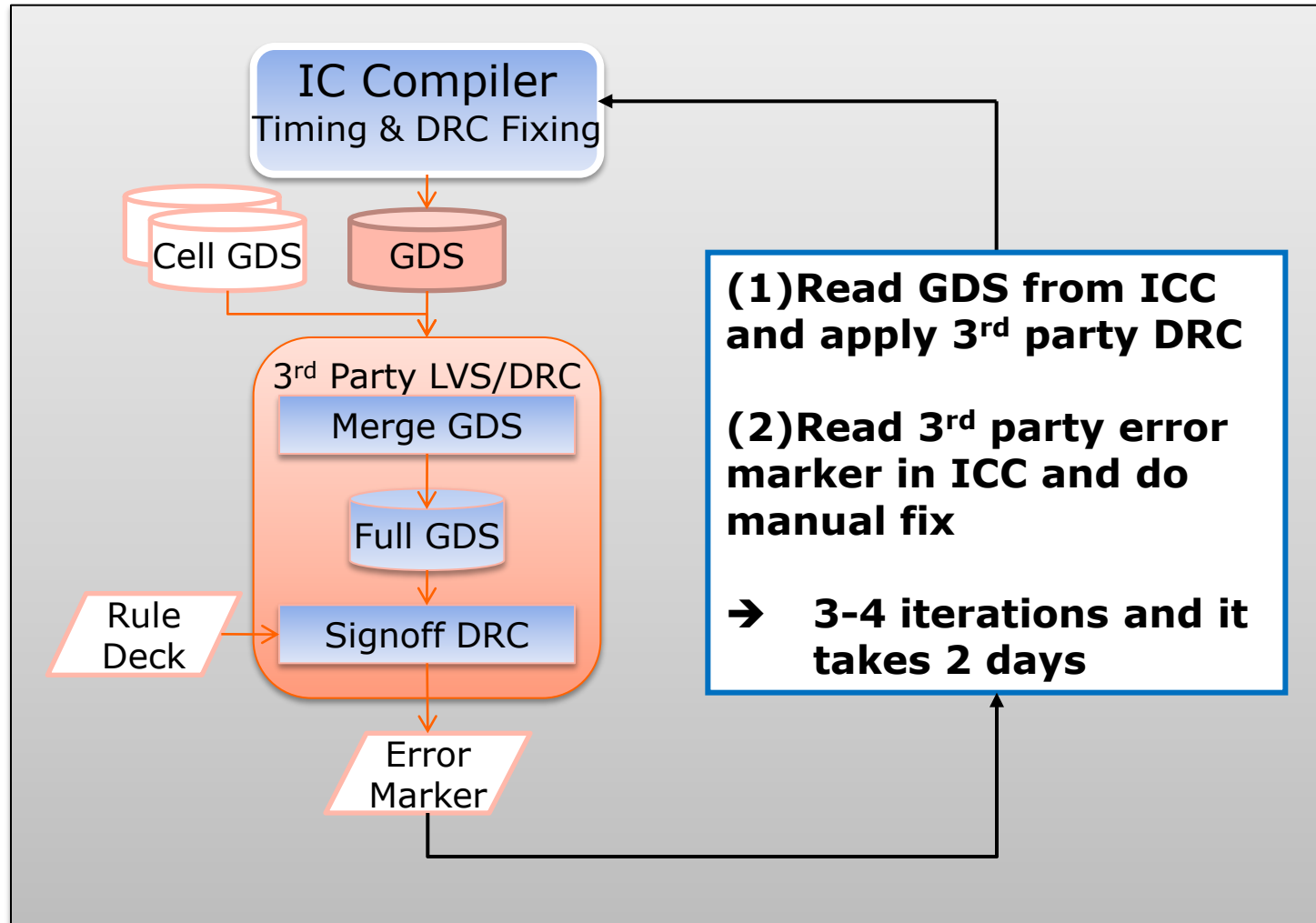
Business Fields

The synergy of our three product segments enables us to rapidly provide optimum solutions.



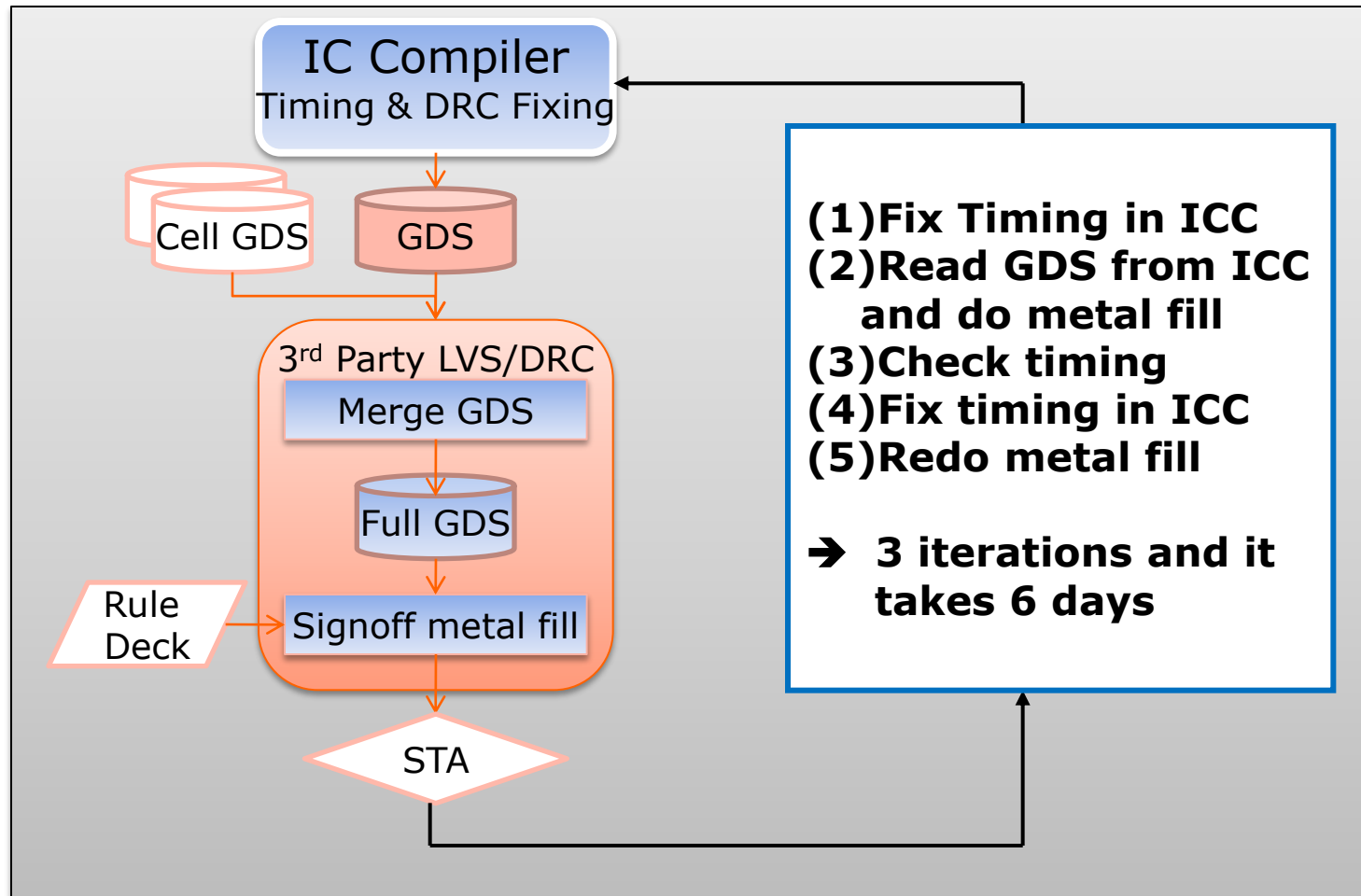
Traditional Physical Verification Flow

Sub-Flow #1 - Signoff DRC Fixing Flow



Traditional Physical Verification Flow

Sub-flow #2 - Signoff Metal Fill Flow



In-Design Physical Verification Flow

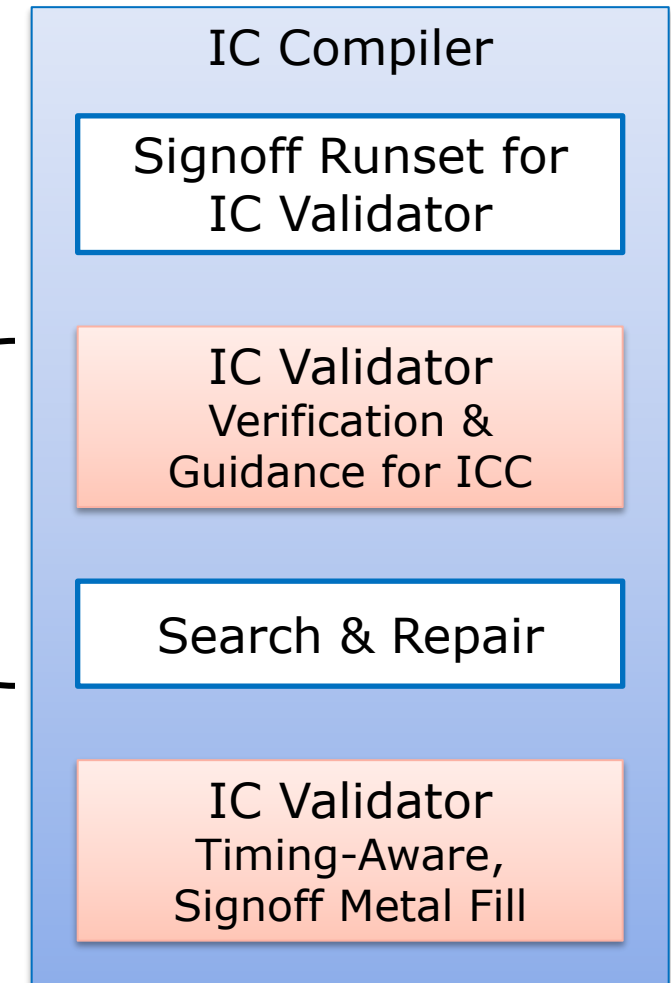
■ Automatic DRC Repair (ADR)

- Delivers sub-flow #1 – signoff DRC
- Faster runtimes for verification and repair
- Correlation to signoff DRC

■ Metal fill

- Delivers sub-flow #2 – signoff metal fill
- Faster runtimes for metal fill insertion
- Timing preserved

ADR



Example #1

In-Design Physical Verification – Automatic DRC Repair

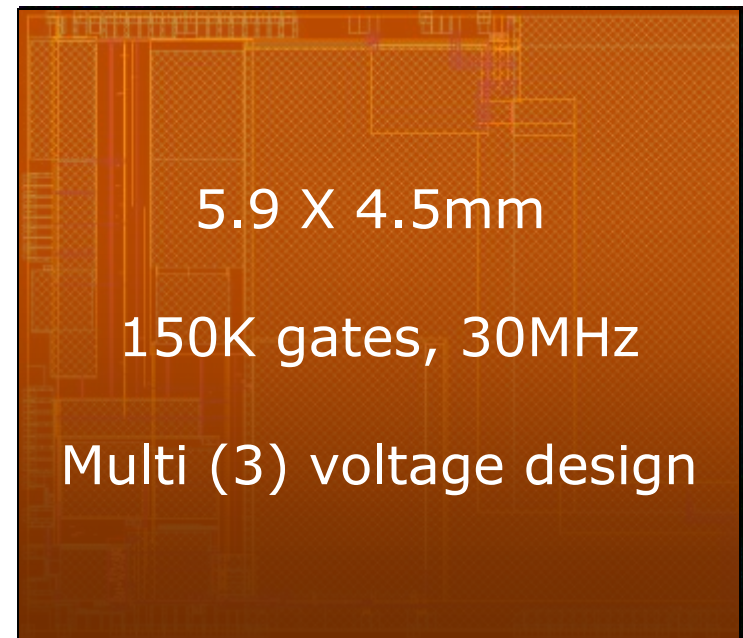
Challenges Using Traditional Flow

1. Short TAT is difficult to meet
➔ From final netlist to tapeout is within a month
2. Special floating metal rule not specified in IC Compiler tech file
➔ We see many DRC errors for this rule

Solution

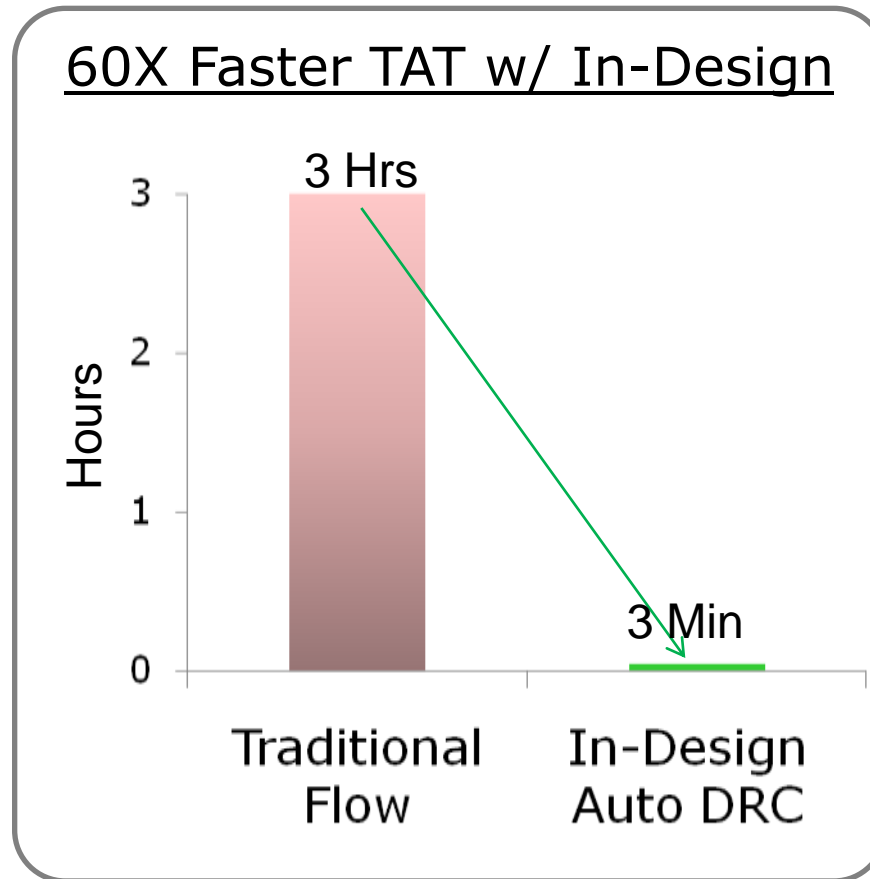
Use In-Design physical verification for automatic DRC repair

Design : MCU



Benefit #1 – Faster TAT For DRC Verification

- Runtime reduction for sign off level verification
- Complete correlation with sign off DRC



ICC and ICV versions qualified in Renesas design kit: ICC: 2009.06 SP5-1, ICV:2009.06 SP1

Benefit #2 – Faster TAT For DRC Repair

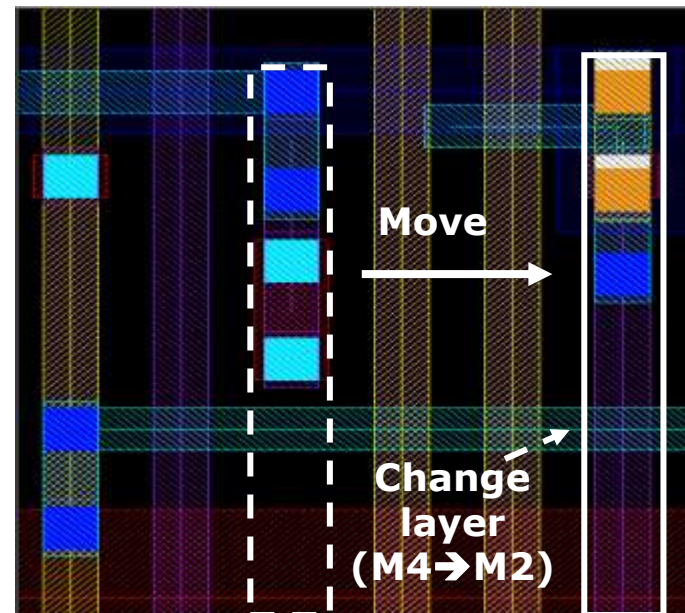
- Violations should be reduced for manual modification

Before ADR



Violation among same layer
(M4) wire segments

After ADR



Wire segments moved and
switched to different layer (M2)
to avoid violation

Automatic DRC repair fixed majority of DRC violations

Example #2

In-Design Physical Verification – Metal Fill

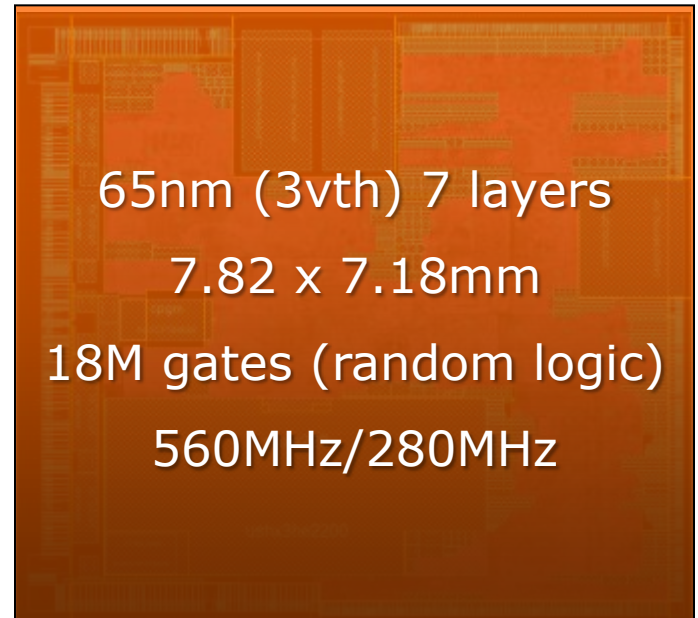
Challenges Using Traditional Flow

1. Big flat design
 - ➔ Run time should be reduced on all steps
2. Timing closure with DFM
 - ➔ Metal filling is necessary for timing analysis

Solution

Use In-design physical verification for run time reduction for metal fill insertion

Design: ASSP



Benefit – Faster TAT

- Drastic run time reduction from traditional flow
 - Multicore function can be used
- Sign off level metal fill insertion, timing preserved

Flow	Number of CPU	CPU Time Hrs:Min:Sec
Traditional	1	33:10:48
In-design	1	9:51:50
	4 (Distributed)	5:06:25

6X Faster TAT vs. Traditional Flow

ICC and ICV versions qualified in Renesas design kit: ICC: 2009.06 SP5-1, ICV:2009.06 SP1

Summary And Next Steps

■ Summary

- Evaluated in-design physical verification and qualified in design kit
- DRC analysis/repair time went from hours to minutes
- Metal fill time went from day to hours while preserving timing
- Released for designers with 2 usage models
 1. Process specific design rule check and auto repair
 2. Metal fill insertion

■ Next Steps

- Evaluate with ICC 2010.03 and ICV 2010.06
 - GDS input / auto DRC repair enhancements for layer switching / window based repair
- Expand process nodes supported
- Add more signoff DRC checks

**In-Design Physical Verification Enables Our #1 Goal
Shorter TAT**