

In-Design Physical Verification For Faster Time To Tapeout

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Physical Design Engineer

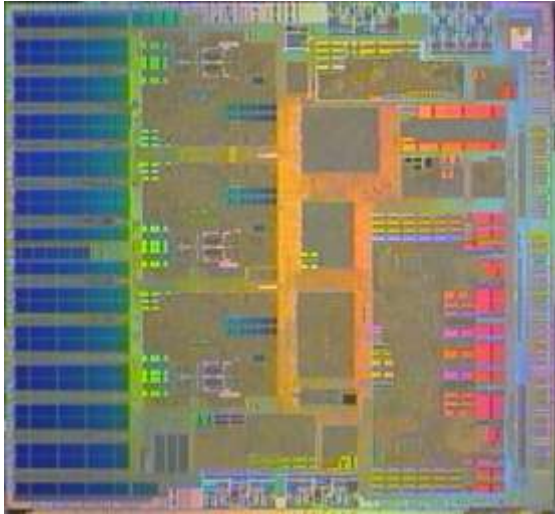
Texas Instruments

14th June 2010

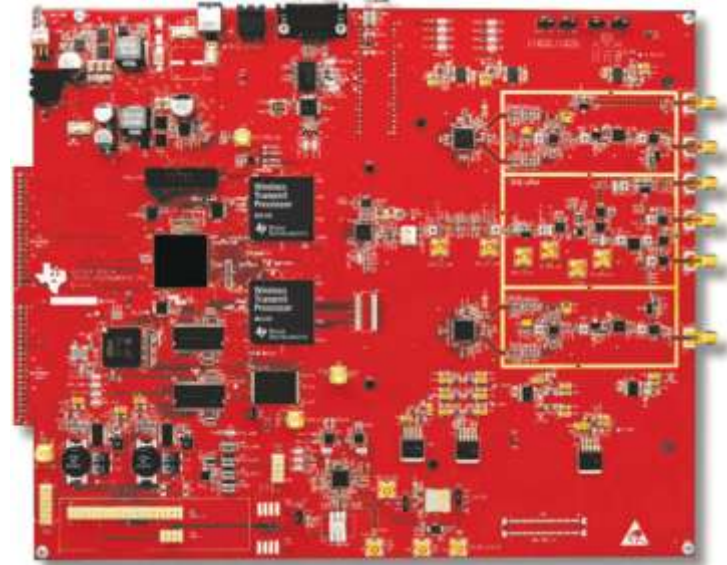
Design Automation Conference

TI Communications Infrastructure Group

Enabling Our Customers to Get Products to Market Quickly

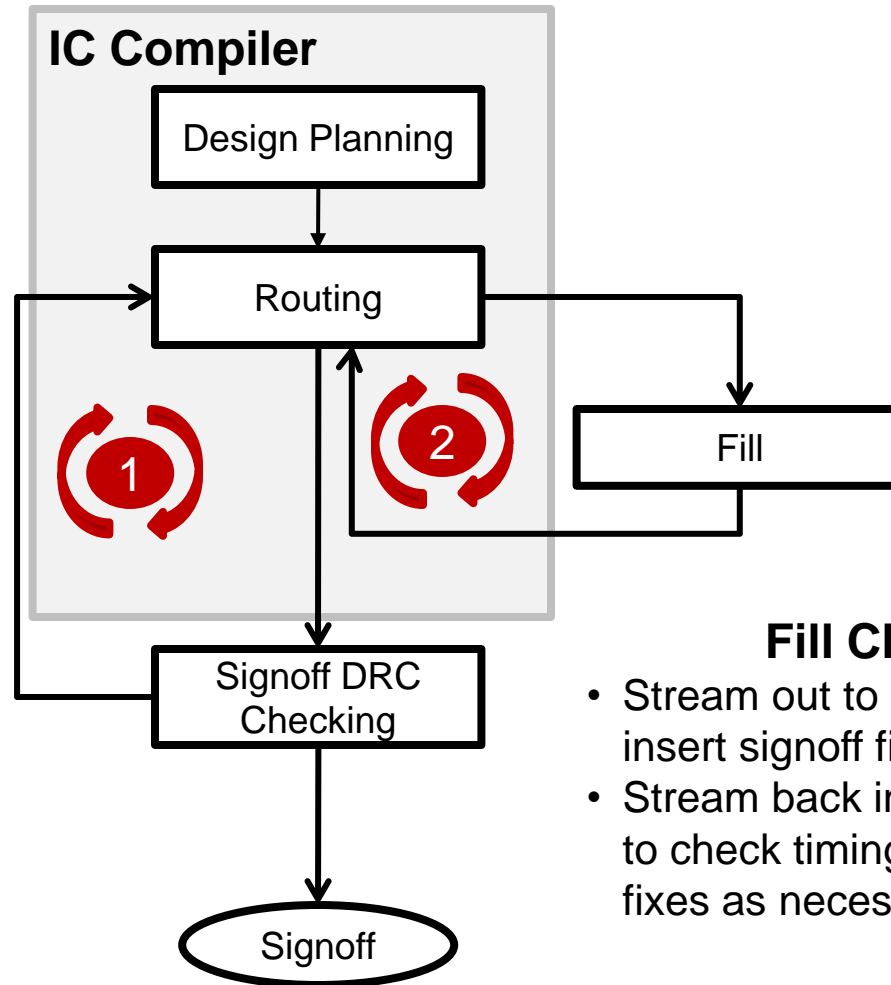


- It all starts with silicon,
- The EDA tools behind it,
- And the ability to converge quickly and predictably



- Need Fast Time to Tapeout!

Iterations In The Earlier Design Flow Caused Tapeout Delays



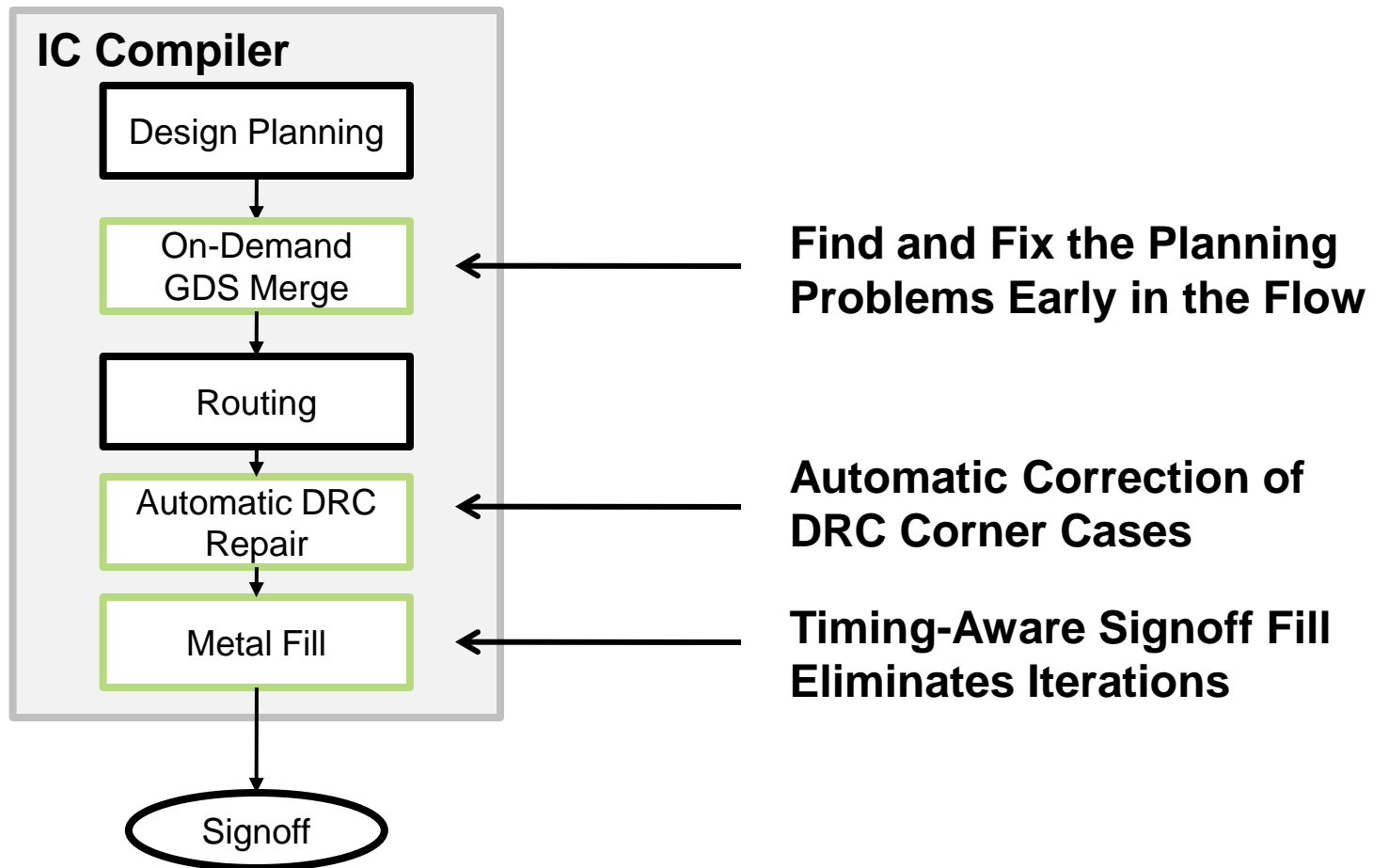
DRC Closure

- Stream out to DRC tool to
 - Any corner cases DRCs
 - Design planning errors that could have been caught earlier
- Stream back in to check timing and make manual fixes

Fill Closure

- Stream out to DRC tool to insert signoff fill
- Stream back in to IC Compiler to check timing and make fixes as necessary

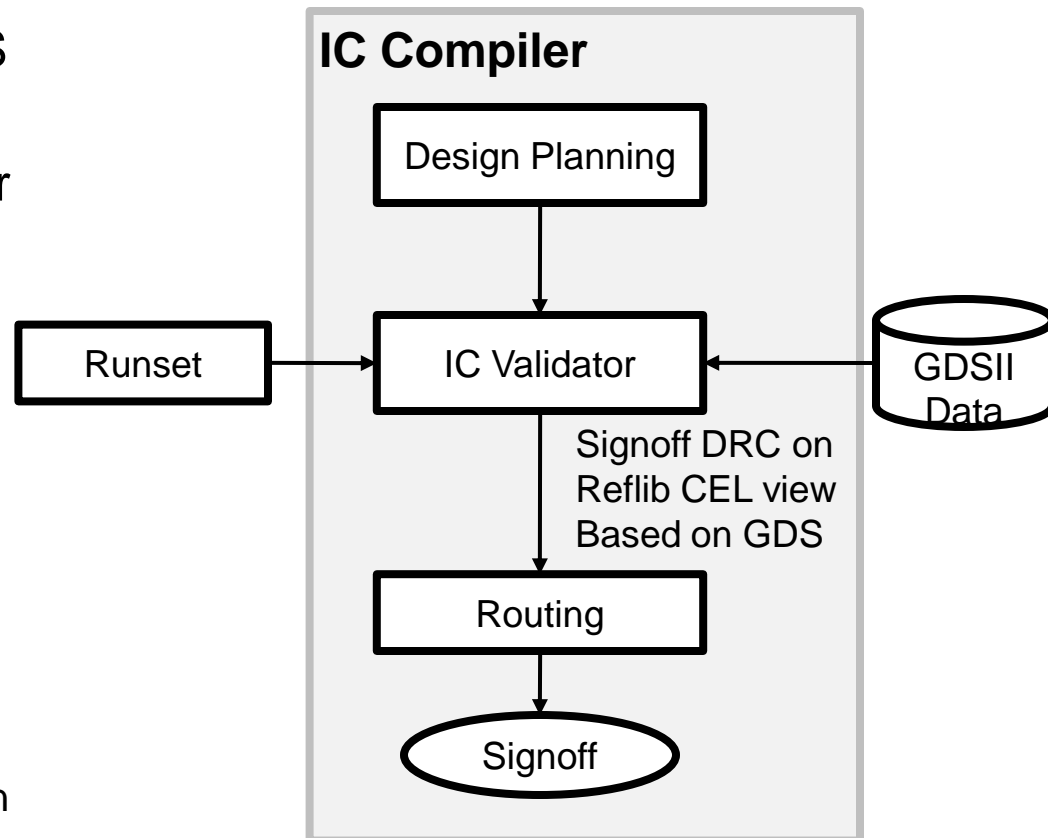
Synopsys In-Design Flow Evaluation to Achieve Faster Time To Tapeout



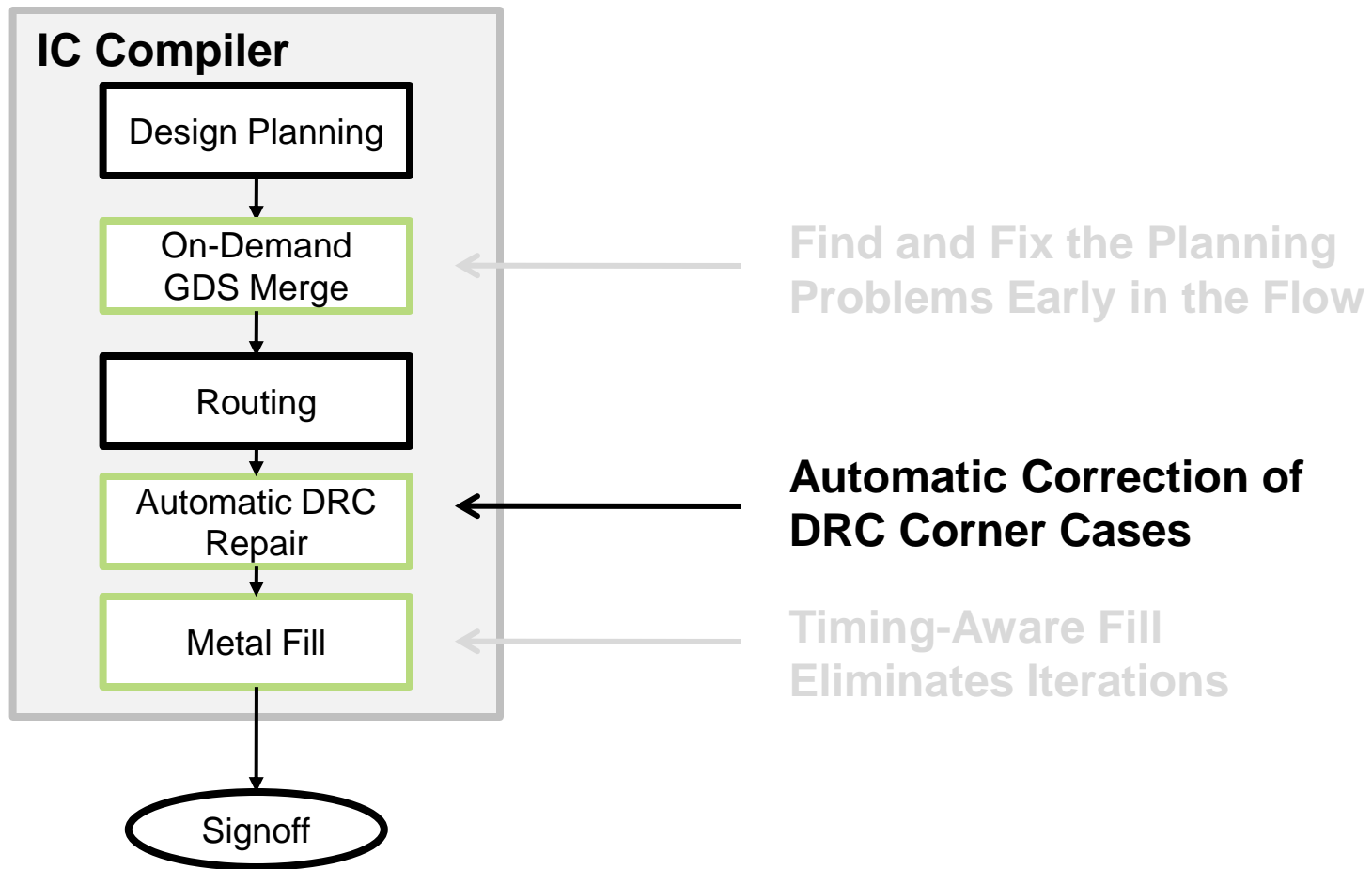
New ICV feature: On-Demand GDS Merge

Flags Errors Earlier In The Flow

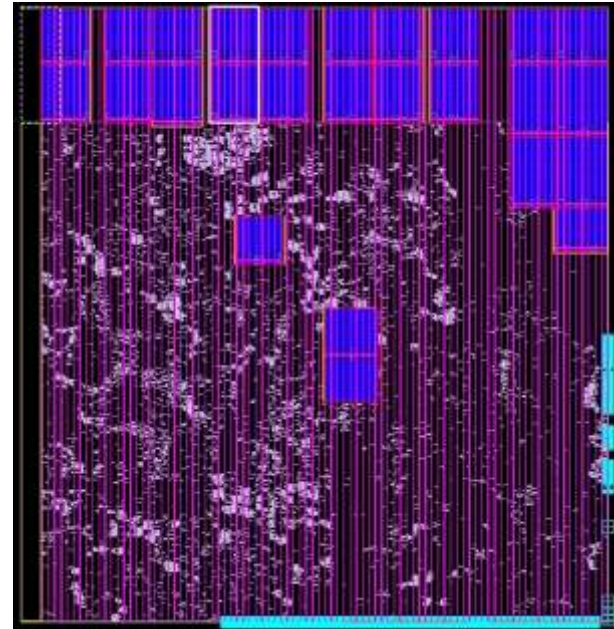
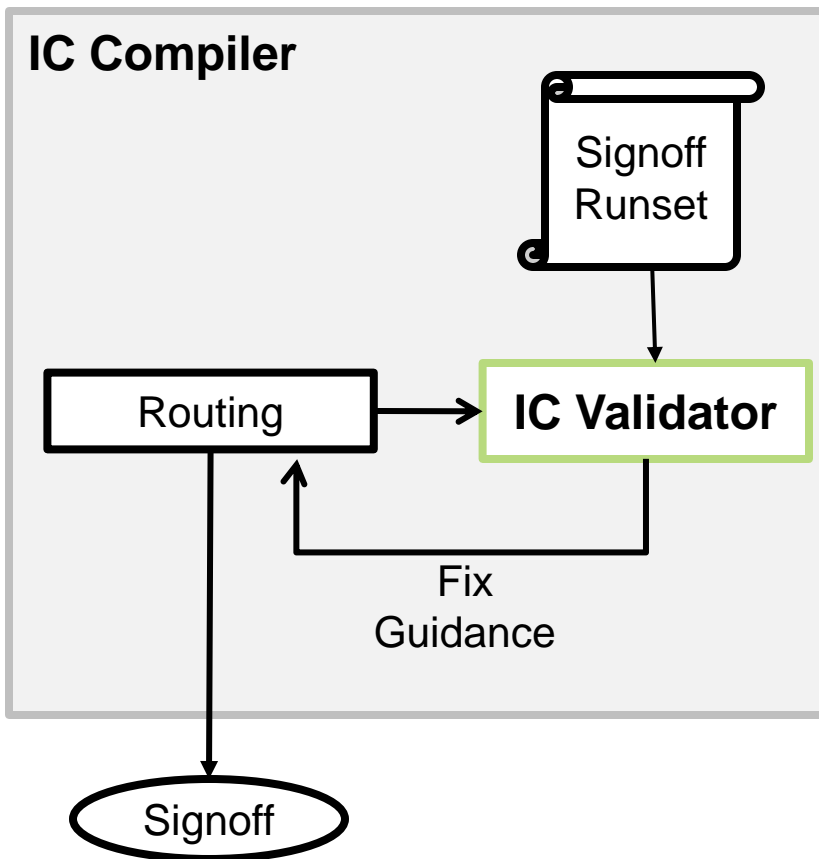
- ICV creates a new MW reflib CEL view from the library GDS
- Does not change the design or existing reference library data
- Benefits
 - Flags base layer errors which would not have been caught by FRAM view based verification
 - Eliminates “out of the flow” GDS merging
 - Newly created reflib CEL view can be re-used in subsequent runs



Synopsys In-Design Flow For Faster Time To Tapeout



Automatic DRC Repair (ADR)



**1.7mmx1.7mm, TSMC 40G
Digital Core, ~30 RAMs
Place and Route in IC Compiler**

**Heavily congested with over 85%
core placement density**

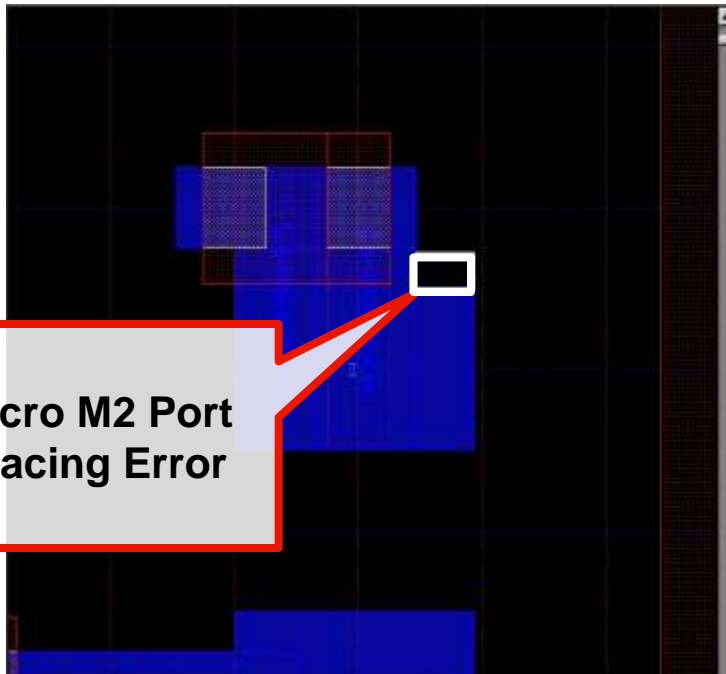
Automatic DRC Repair Results

Sign-off DRC Rules	Errors Before ADR	Errors After ADR	Fix Rate
M2.S.5 : Space at Mx line-end => 0.10	84	0	100%
M3.S.1 : Space >= 0.07	6	0	100%
M3.S.5 : Space at Mx line-end => 0.10	12	0	100%
M2.S.1 : Space >= 0.07	21	2	90% Heavy Congestion

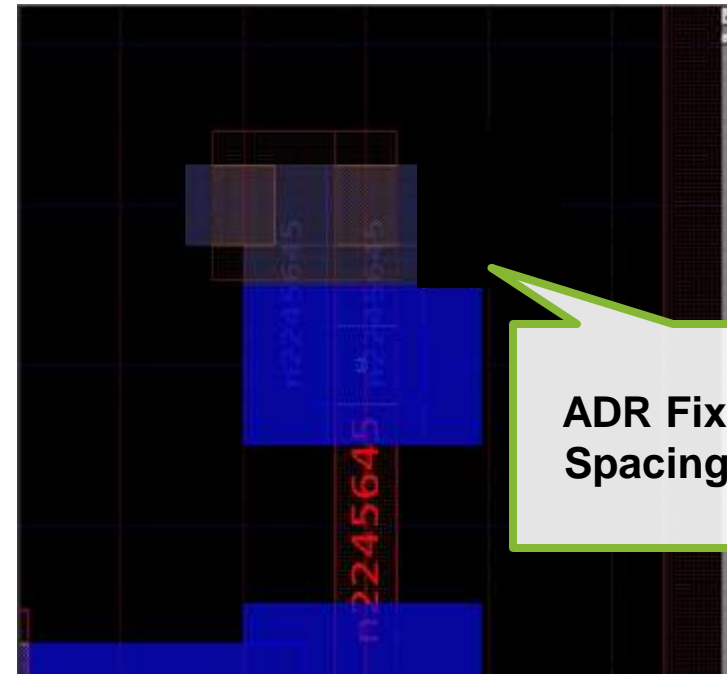
Example #2 - Automatic DRC Repair

M2.S.1 Spacing (After GDS Merge Flagged Error)

Original Design



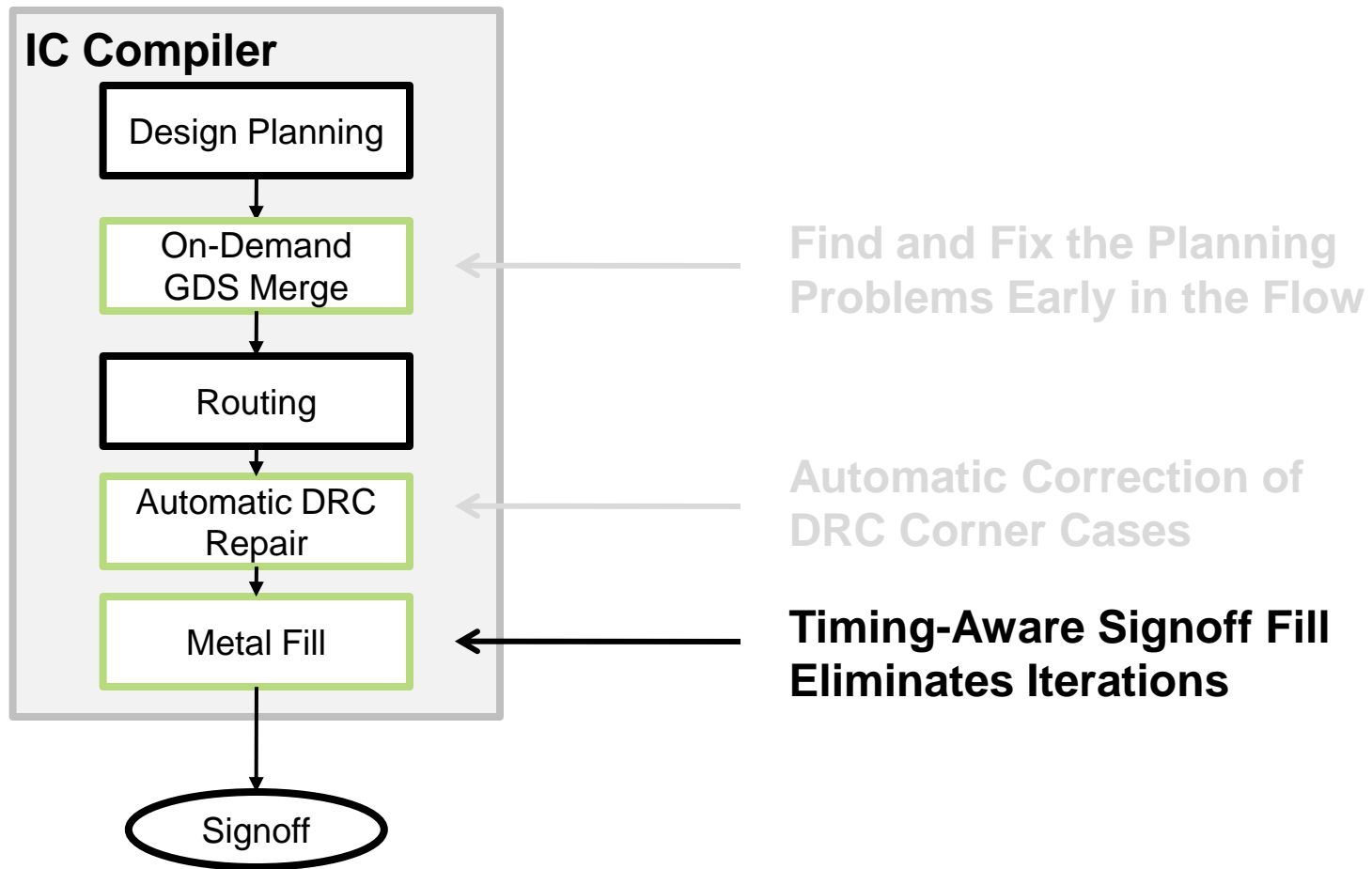
Fixed Design



Macro M2 Port
Spacing Error

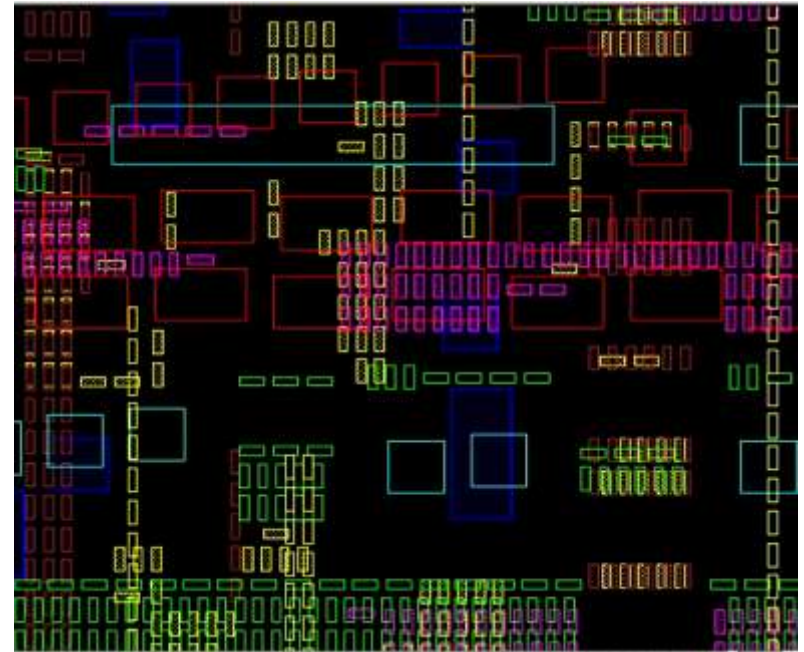
ADR Fixed M2
Spacing Error

Synopsys In-Design Flow For Faster Time To Tapeout



Timing-Aware Metal Fill

- IC Compiler command (`signoff_metal_fill`) allows designer to populate IC Compiler FILL view
- Fill is correct by construction, since it is created using the foundry metal fill deck
- Timing aware options:
 - Allow user to block fill around nets on critical paths
 - User can also provide a list of critical nets



In Conclusion

Current In-design Status

- In-design Metal Fill deployed at 40nm
- Automatic DRC Repair & On-Demand GDS Merge for future designs
 - ADR ~3x faster than the manual flow
 - It fixed all but 2 of my 123 violations
 - It ran while I was asleep

Recommendations to Synopsys

- Select rule/layer base ADR to reduce the turn around time
- User control over # of iterations for early look at ADR performance
- Fixing the power net violations created by the Pre-Router

In-Design Physical Verification has saved us significant cycle design time