

Power Compiler

Automatic Power Management within Galaxy™ Design Platform

Overview

Reducing power consumption is required in today's semiconductor designs. Silicon technology advances have made it possible to pack millions of transistors switching at high clock speeds on a single chip. While these advances bring unprecedented performance to electronic products, they pose difficult power dissipation and distribution problems. These problems must be addressed, because consumers demand longer battery life in addition to lower cost in computers, battery-operated systems, medical devices, telecommunications equipment and many high-volume consumer products.

Power Management

A key to successful power management is automatic power reduction. This enables designers to meet their power budgets without adversely affecting their productivity or time to market. Power Compiler's push-button power reduction capabilities at the Register Transfer Level (RTL) and gate level are fully integrated with Synopsys' Galaxy™ design synthesis and physical design flow.

Power Compiler

Power Compiler™ automatically minimizes power consumption at the RTL and gate level. At the RTL, during the design elaboration phase, Power Compiler performs automatic clock gating to reduce the power consumption. At the gate level, driven by the design constraints, it performs simultaneous optimization for timing, power and area. It supports multithreshold libraries for automatic leakage power optimization. Power Compiler is seamlessly integrated with the synthesis design flow and shares the same GUI, commands, constraints and libraries with the Design Compiler® and Physical Compiler® tools.

Power Compiler: RTL Power Optimization

Synopsys' Power Compiler performs automatic clock gating at the RTL without requiring any changes to the RTL source. This enables fast and easy trade-off analysis and maintains technology-independent RTL source. Clock gating is a common power

reduction technique used manually in many power-critical designs. Power Compiler's clock gating is complementary to manual clock gating done at the block level. It gates the clocks of individual synchronous load-enable register banks instead of circulating the output back to the input when the load-enable condition is invalid. Power Compiler automates this technique during the design elaboration phase, without requiring any additional effort from the design engineer. When applicable, substantial power savings can be achieved – up to 70 percent or more – at the block level.

Power Compiler: Gate-Level Power Optimization

At the gate level, Power Compiler delivers further push-button power reduction. It delivers an average of 10 to 20 percent reduction in power during gate-level optimization without violating timing constraints. Based on the user's timing, power and area constraints, Power Compiler measures trade-offs between positive timing slacks, area and power and then delivers the lowest-power-consuming design that meets timing constraints, while maintaining the area limit when specified by the user. The push-button power optimization at the gate level reduces the dynamic power as well as the leakage power, which is the majority of the power consumed when the device is in standby mode. Power Compiler shares the same GUI, shell, and compile commands with Design Compiler and Physical Compiler. It is fully integrated with Design Compiler and the existing design flow.

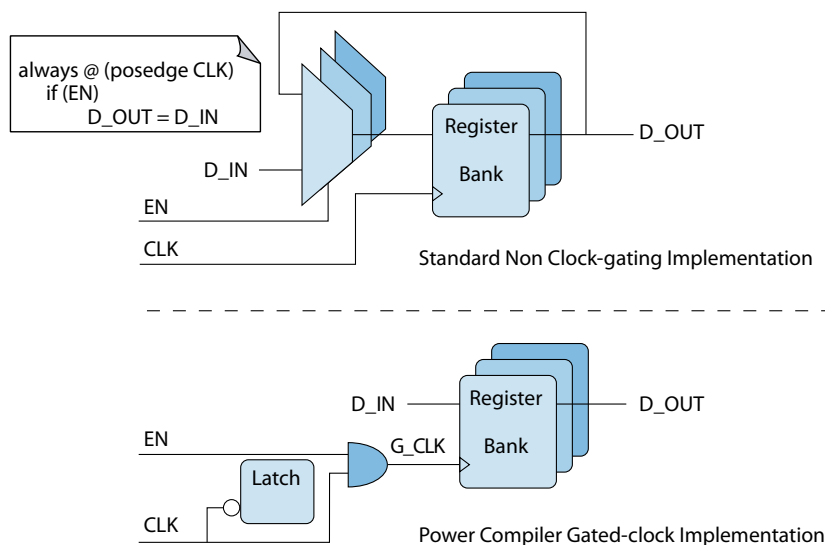


Figure 1: Power Compiler RTL clock-gating needs to be set as a constant 0 to disable test.

It uses synthesis libraries that are used by Design Compiler and are enriched with power information. Over 30 silicon and library vendors, as well as the commercially available characterization tools, generate the power information for Power Compiler and incorporate this information into the synthesis libraries.

Power Modeling Capabilities

Power Compiler uses a robust power model to estimate and control three components of power consumption: switching (capacitive) power; internal (short circuit) power, and leakage (static) power. Switching or capacitive power, which typically represents 60 to 80 percent of power consumption, is the power dissipated when a load capacitance is charged or discharged, i.e., 0-to-1 or 1-to-0 transitions of the nets in the design. Internal or short circuit power, typically 20 to 40 percent of power consumption, is the power consumed within a cell. This includes short circuit (V_{dd} to ground) as well as all power dissipated due to switching of internal nets. The internal power model is provided in the form of internal energy look-up tables. This internal power model supports multiple energy look-up tables per cell, based on input and output pin states, as well as pin-to-pin power arcs.

Leakage, or static power, is the power dissipated due to sub-threshold leakage and the current flow through the reverse-biased p-n junction between diffusion and substrate. Leakage power accounts for the majority of power dissipated when the circuit is inactive—an important metric to measure and optimize for battery-powered applications. Power Compiler accurately evaluates gate-level trade-offs to minimize these three power components. The library information needed to analyze and optimize power is already contained in the synthesis libraries provided by most of the major library vendors, and can be generated using most of the commercially available library characterization tools.

This comprehensive power model can be used to accurately model the power consumption of memories, I/Os and complex cells. For example, the power consumption of a memory during read-write cycles can be modeled based on the state of the read-write mode bit.

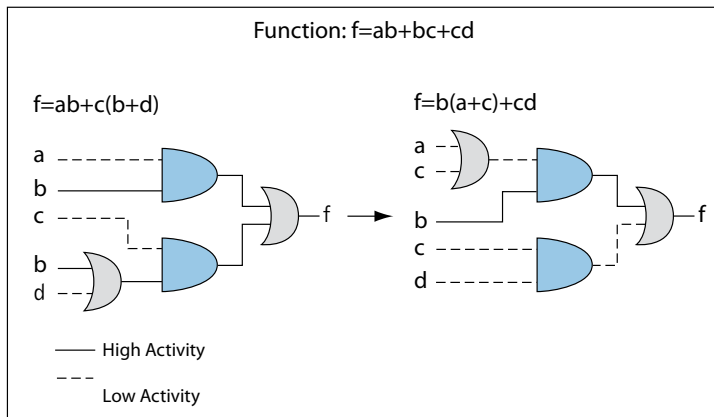


Figure 2: Factoring technique for reducing the circuit switching activity.

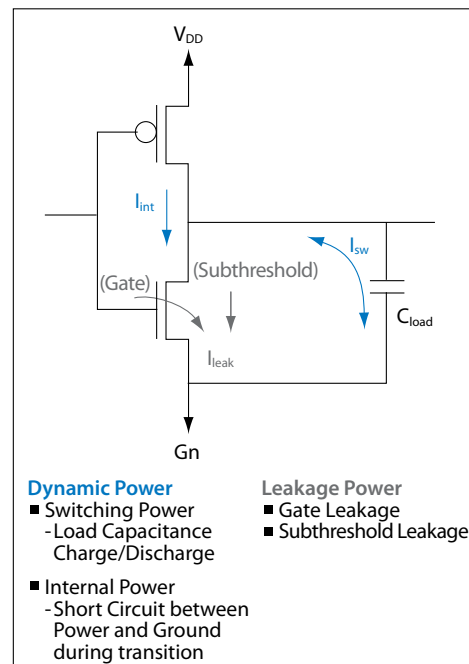


Figure 3: Power dissipation in CMOS designs.

Synopsys Advantage

The Synopsys Power Management Solution for the design flow gives designers a powerful arsenal of tools to optimize, estimate, analyze and manage today's shrinking power budgets. Design engineers who are serious about providing power-efficient, cutting-edge technology to their customers will easily see the value in handling power problems early in the flow. By understanding a design's power requirements at every phase of the design cycle, engineers will be able to produce high-performance, power-sensitive products without impacting cost or time to market.

For a complete directory of Synopsys' available Power Solutions visit: www.synopsys.com/galaxypower.



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