White Paper

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Understand and Avoid Electromigration (EM) & IR-drop in Custom IP Blocks

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Abstract

Advances in process technology and changing design styles are increasing the impact of electromigration (EM) and IR-drop effects on the performance and reliability of analog, mixed-signal, memory and custom digital IP blocks at 28nm and below. In this white paper, we discuss the various trends exacerbating EM and IR-drop effects as well as design and analysis techniques to avoid them, and introduce Synopsys' transistor-level analysis solution, which includes CustomSim™ for FastSPICE circuit simulation, StarRC™ for extraction, and Galaxy Custom Designer® for custom layout.

Nanometer Technology Trends

What general technology trends are contributing to the significance of EM and IR-drop effects in modern IC designs? Figure 1 provides examples of three distinct trends. Firstly, driven by Moore's law, metal interconnect widths are decreasing exponentially. As a result, the overall cross-sectional area of interconnect is shrinking. Secondly, with increasing integration of functionality and passive devices the total interconnect length is exploding as well, which means that there are more wires on a die that are susceptible to EM effects. Finally, currents are not scaling proportionally to shrinking wire widths and, therefore, modern ICs have extremely high current densities.

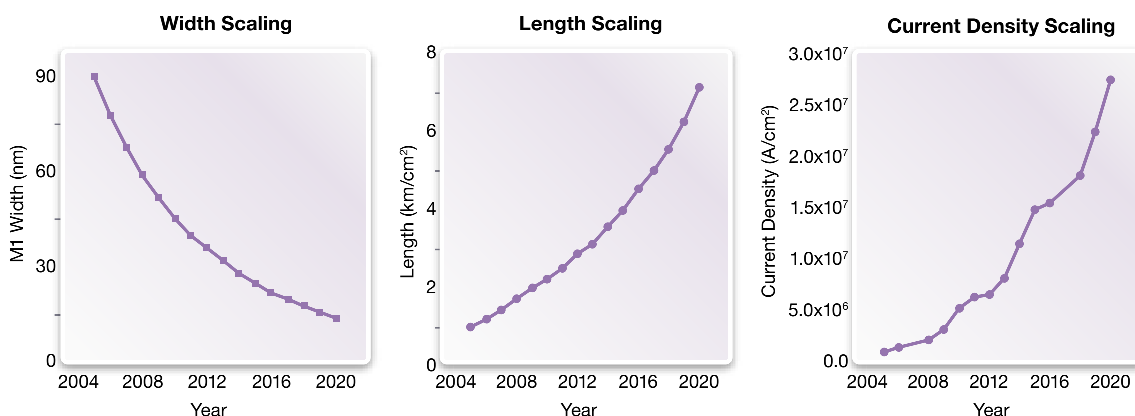

Figure 1: Nanometer technology trends

What is Electromigration?

Electromigration is the gradual displacement of metal atoms in a semiconductor. It occurs when the current density is high enough to cause the drift of metal ions in the direction of the electron flow, and is characterized by the ion flux density. This density depends on the magnitude of forces that tend to hold the ions in place, i.e., the nature of the conductor, crystal size, interface and grain-boundary chemistry, and the magnitude of forces that tend to dislodge them, including the current density, temperature and mechanical stresses.

Failure Mechanisms

There are two different EM failure mechanisms that occur due to asymmetry in the ion flow. The first example in Figure 2 shows a void where the outgoing ion flux exceeds the incoming ion flux, resulting in an open circuit. The second example shows a hillock where the incoming ion flux exceeds the outgoing ion flux, resulting in a short circuit.

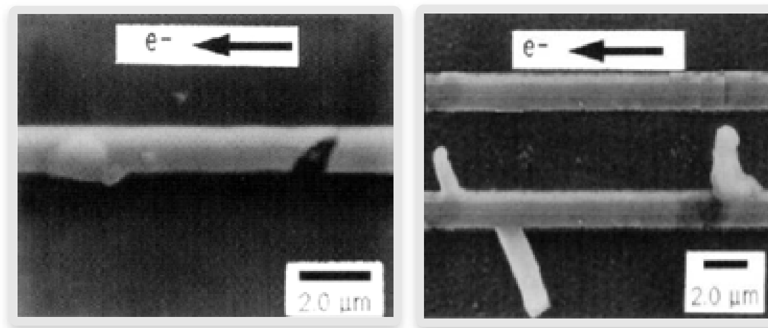

Figure 2: Void (open circuit) and hillock (short circuit)

History of Studies into Electromigration

The EM phenomenon was originally discovered by a lesser-known French scientist named Gerardin over 100 years ago. It only became of practical interest in 1966 with the introduction of the first ICs. A number of research activities were undertaken in the 1960s, the most significant of which was one undertaken by Jim Black at Motorola in 1969. A result of Black's work was an equation that is used to determine the mean time to failure (MTTF) of a metal wire when subjected to EM effects, as shown below:

$$MTTF = \frac{A}{J^N} . \exp\left(\frac{E_a}{k.T}\right)$$

Where the parameters of the equation are defined as:

A	Cross-section area-dependent constant'
J	Current density
N	Scaling factor, usually set to 2
E_a	Activation energy for electromigration
k	Boltzmann constant
T	Temperature

The current density is one of the few parameters that are under the designer's control.

Electromigration Dependency on Physical Effects

Temperature

From Black's equation it is clear that failure due to electromigration is dependent on temperature, however, there is a more sinister dependence on temperature that accelerates failures due to voids. Figure 3 highlights a cyclical positive feedback loop that ultimately ends in failure.

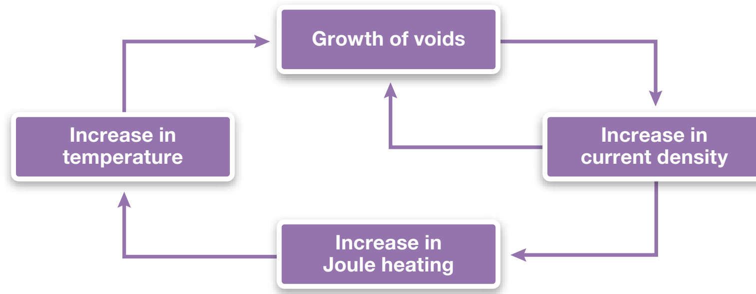

Figure 3: Electromigration dependency on temperature

Once a void begins to develop in a metal wire, the wire itself becomes narrower at that point. Due to the reduction in width, the current density increases and, therefore, the interconnect temperature increases due to Joule heating. Joule heating is a result of root-mean square (RMS) current. As the temperature of the wire increases, the growth of the void accelerates, and eventually an open circuit occurs. This is why it is critical to also take RMS current into account when performing EM analysis.

Wire Width

Current density is the primary factor influencing electromigration. By increasing the wire width, current density is reduced and susceptibility to EM is reduced. There is one exception to this rule and that is when the wire width falls below the average grain size of the interconnect material. This apparent contradiction is caused by the position of the grain boundaries, which in such narrow wires lie perpendicular to the width of the whole wire. Because the grain boundaries in these so-called “bamboo structures” are at right angles to the current, the boundary diffusion factor is excluded, and material transport is correspondingly reduced.

However, the maximum wire width possible for a bamboo structure is usually too narrow for signal lines of large-magnitude currents in analog circuits or for power supply lines. In these circumstances, slotted wires are often used, whereby rectangular holes are carved in the wires. Here, the widths of the individual metal structures in between the slots lie within the area of a bamboo structure, while the resulting total width of all the metal structures meets power requirements.

Wire Length

There is a lower limit for the length of interconnect that will be subjected to the effects of electromigration. It is known as “Blech length”, and any wire that has a length below this limit will not fail by electromigration. Here, a mechanical stress buildup causes a reversed migration process which reduces or even compensates the effective material flow towards the anode. Figure 4 depicts these so-called “immortal” wires.

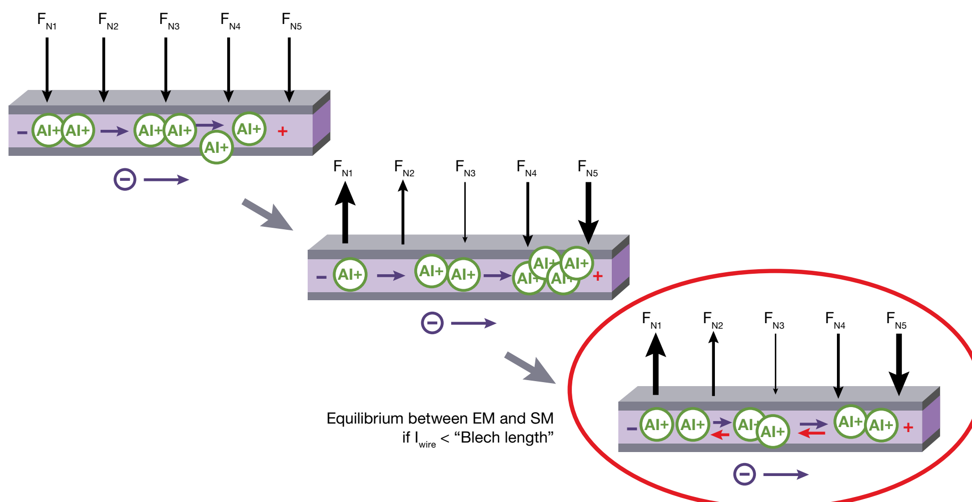

Figure 4: Illustration of “Blech length”

Impact of Physical Layout

Interconnect layout has an impact on electromigration and current density. Aside from wire width, there are particular layout strategies one can use to minimize EM effects. The objective behind these strategies is to achieve homogenous current flow[1]. Figure 5 shows two different layout strategies to achieve homogenous current flow. Firstly, 90° corners and rapid wire width reduction should be avoided. The current crowding and rapid increase in current density exacerbate EM. The right-hand image shows how critical via arrangement is to ensure homogenous current flow.

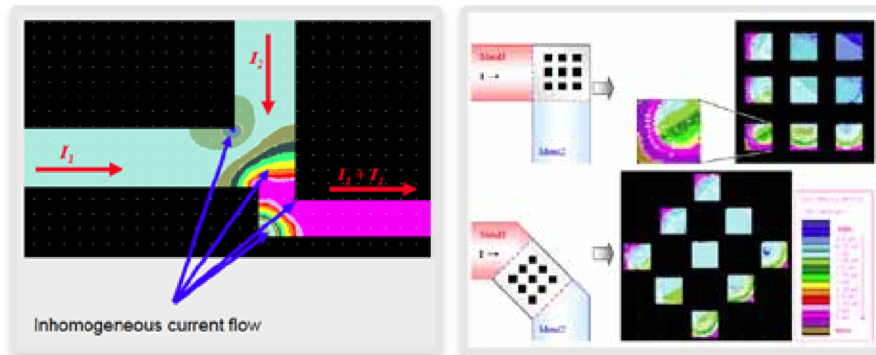

Figure 5: Layout strategies to minimize EM

EM Rules for Nanometer Processes

Modern nanometer process technologies have very complex rules for current density limits that are not only dependent on wire widths but the length of wire, as well as the dimensions of the wire layers above and below a via layer. Tables 1 and 2 demonstrate the complexity of metal and via EM rules[2].

Layer	Metal Length (µm)	Metal Width (µm)	I_{max} (mA)
Mx	L ≤ A	Any width	4*(em_coef)*width
	L > A	W ≥ B	2*(em_coef)*width
	L > A	W < B	1*(em_coef)*width

Table 1: Example of metal layer EM rules

Layer	Bottom Metal Length, Width (µm)	Upper Metal Length, Width (µm)	I_{max} (mA)
Mx	L ≤ A; any width	L ≤ A; any widths	4*(VIA_em_coef) per via
	L > A; W ≥ B	L ≤ A; any width	2*(VIA_em_coef) per via
	L ≤ A; any width	L > A; W ≥ B	2*(VIA_em_coef) per via
	L > A; W ≥ B	L > A; W ≥ B	2*(VIA_em_coef) per via
	Others	Others	1*(VIA_em_coef) per via

Table 2: Example of via layer EM rules

Synopsys' CustomSim reliability analysis solution provides support for flexible TCL-based rule creation that enables designers to capture these complex nanometer EM rules. The TCL interface enables the creation of procedures to calculate RMS as well as average and peak current values that can then also be used to verify the individual rules.

Synopsys CustomSim Reliability Analysis Solution for Custom IP Blocks

Synopsys offers a comprehensive reliability analysis solution that offers a combination of static and dynamic analysis for power and signal net EM and power net IR-drop.

Static Net Resistance Check

Before performing a complete dynamic simulation for measurement of IR-drop effects, a quick DC analysis of power and ground bus resistance can be used to catch gross errors such as missing vias and undersized metallization. CustomSim determines the resistance from each external power pad connection to the power pins of internal blocks, generating text reports and GDSII resistance maps for graphical visualization of power and ground bus resistance through all metal and via layers. The analysis results can be visualized in Custom Designer LE and all resistance paths can be cross-probed and debugged.

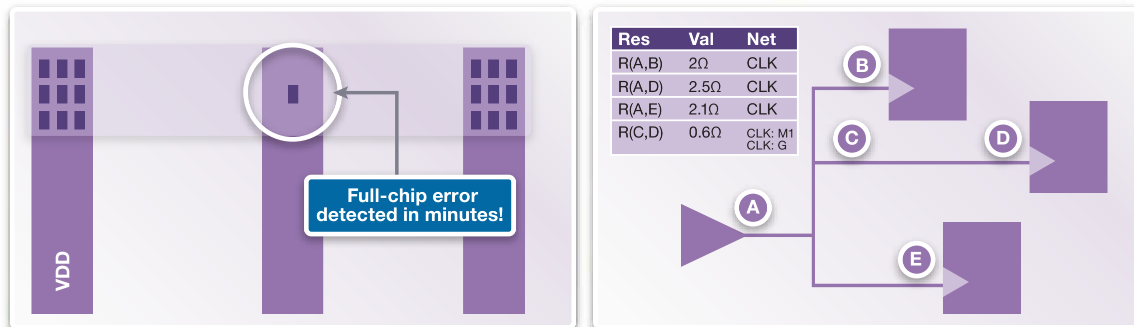

Figure 6: Static power and signal net resistance check

Dynamic EM/IR-drop Analysis

CustomSim has the capability to analyze IR-drop and electromigration in power and ground busses, while simultaneously accounting for the effects of interconnect resistance on dynamic circuit performance. The unique direct-coupled methodology provides highly accurate measurement of power bus currents by performing full-circuit simulation in the presence of back-annotated parasitics. CustomSim overcomes the limitations of simulation with millions of extracted parasitic resistors, by incorporating built-in compression and reduction algorithms to maintain accuracy, capacity and performance.

Using this direct-coupled methodology, accurate transient current waveforms are acquired during dynamic simulation and are used for detailed measurement of IR-drop and current density in the complete, unreduced power and ground nets. An alternative approach to power-net analysis supported by CustomSim estimates IR-drop by characterizing cells before they are placed into a circuit layout. Graphical output in GDSII and other formats allows designers to overlay results on their layout design for analysis and debug.

CustomSim calculates current densities in narrow signal nets to determine their susceptibility to EM. Bidirectional current flow is correctly considered, including calculation of the RMS currents required for monitoring Joule heating within the design. These results are presented as GDSII files for physical visualization. CustomSim can include all of the design's extracted coupling capacitors in addition to the grounded capacitors. This provides a high level of precision in determining the current entering or leaving segments of signal net interconnect, enhancing the quality of results.

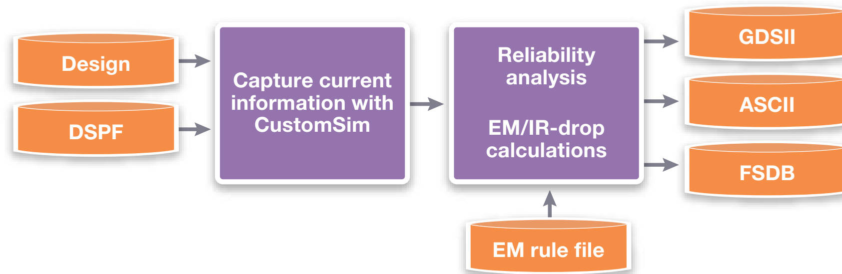

Figure 7: Dynamic reliability analysis flow

Visualization in Custom Designer LE

CustomSim reliability analysis is uniquely integrated with Custom Designer LE to provide designers with the ability to annotate and debug reliability results in the layout editor. Pictured on the right of Figure 8 is the browser that is used to organize results and, if needed, modify the layer binning. With this integration, designers can easily locate and pinpoint reliability results on supply net wires and browse and filter violations in the layout editor.

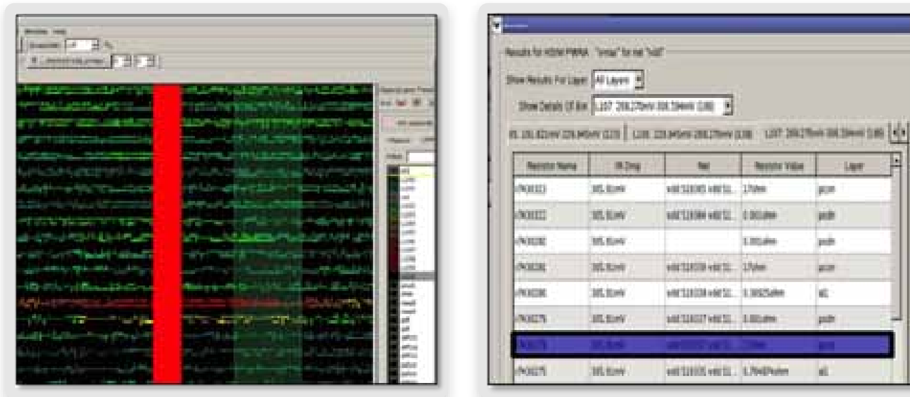

Figure 8: Visualization of EM and IR-drop results in Custom Designer LE

Conclusion

The trend in nanometer technologies underscores the need for electromigration to be taken into account for all custom IP blocks. EM rules themselves are growing in complexity with additional dependencies on length and width. Synopsys' CustomSim reliability analysis solution provides the flexibility to support these complex rules, as well as to conduct EM analysis with RMS, average and peak currents. A static net resistance check is provided for designers to run a quick sanity check to identify any mistakes in layout due to missing vias or narrow wires.

References

[1] "An Introduction to Electromigration Aware Physical Design", J. Lienig, Proc. of the Int'l Symposium on Physical Design (ISPD), April 2006

[2] "Hybrid IR/EM Analysis Flow with EM Rule Extension", Gary Chan, TSMC; 2011 Synopsys User Group (SNUG) Conference, Taiwan

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