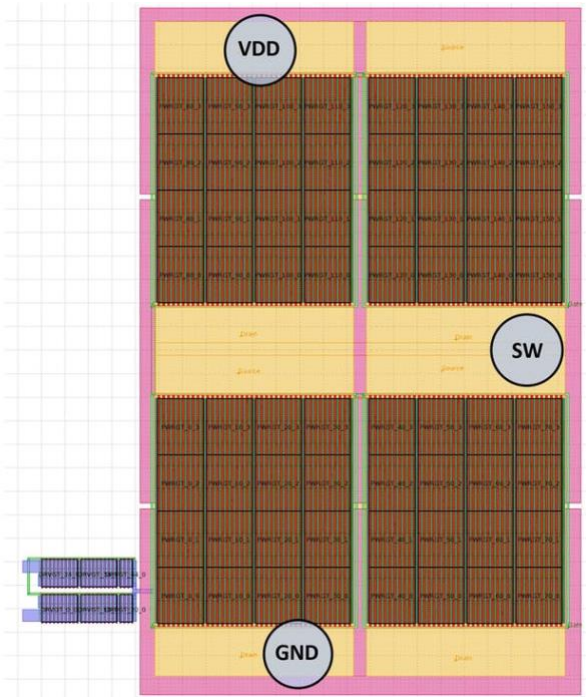
Efficient Power Semiconductor Devices – A Critical Success Factor for Today's Low Power Electronics

Integrated Circuits (ICs) are ubiquitous in our daily lives, from communication devices to transportation systems, it touches every aspect of our existence. The advancements in semiconductor technologies and power management techniques are one of the key contributor to this trend. Power semiconductor devices drive and manage the distribution and quality of power, an essential workhorse behind IC and system operations. These devices provide conversion and control of power, thus driving the efficiency and reliability of power delivery to the system.

However, as IC complexity increases with higher silicon density, smaller geometry, faster performance, and lower operating power, the ability to accurately predict the chip and systems' behavior prior to tape-out becomes a major design challenge. The layout of a large-area power device is a very complicated system, containing thousands or even millions of elements. Power devices today require very low ON-resistance (RDS_{on}), just a few milliohms. The ability to understand the effects of non-uniform layout and complex current flow patterns, as well as the impact of the surrounding circuitry is essential in accurately predicting the devices' behavior.



Seemingly reasonable real-world layout can contain potential reliability problems, non-uniform switching issues, lost efficiency, overly large dead times, EM violations, voltage-drop issues and damaging shoot-through current.

Designing today's power semiconductor devices require a comprehensive design and optimization solution. Traditional parasitic extraction tools or field solvers are unable to handle realistic layouts due to their size and geometry complexities or the multi-dimensional nature of the current flow. Using automated rule check and layout-versus-schematics systems (DRC, LVS) may miss layout problems such as discontinuities, current crowding, or excessive potential drops. On the other hand, analytical and spreadsheet models, while being useful, cannot accurately capture the complexity of top metal layouts that are constrained by the package, wire bonding, or ball-array requirements.

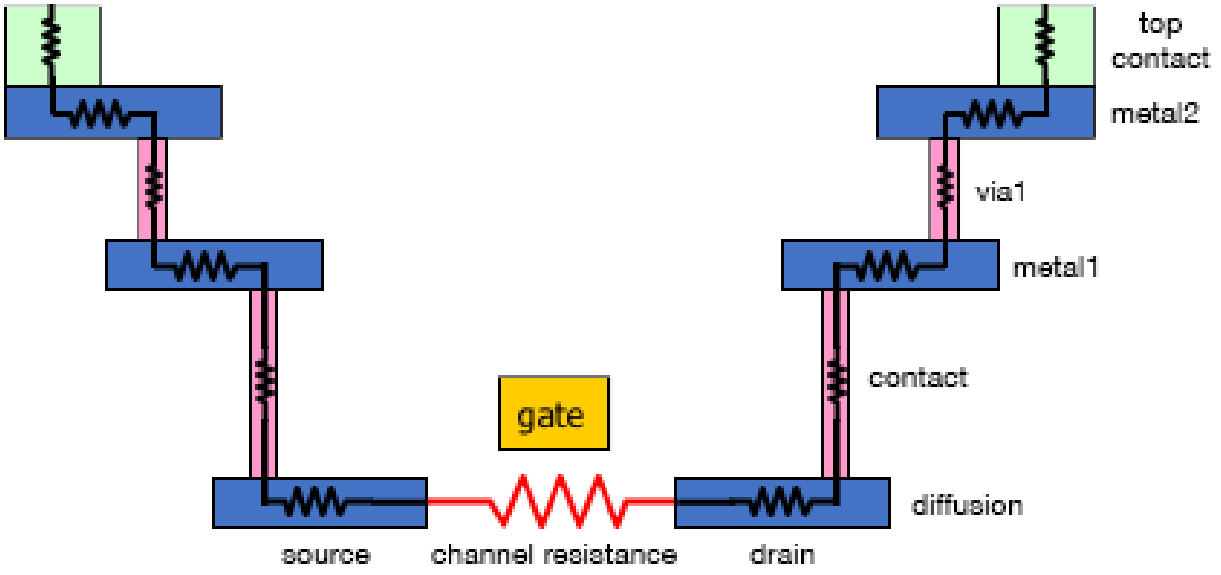
In order to increase efficiency, reduce the probability of an error, and drastically speed up and improve the quality of layout design, today's engineers need to deploy an extraction, analysis and optimization solution that can address the following needs:

- Automated and accurate calculation of large area device RDS_{on} value
- Current density and potential distribution analysis and its impact on electromigration
- Effective design and location of current sense devices
- Optimization of layout across area and reliability for balanced design
- Easy to use interface with quick feedback and what-if analysis

Automated RDS_{on} Calculation

A typical challenge faced by engineers or power device designers is to understand the contribution of each resistive component such as metal layers, vias, contacts and device/channel to the total ON-resistance (RDS_{on}). The answer to this challenge is important in focusing proper efforts on layout optimization. Being able to quickly and accurately identify the area of high resistance allows engineers to effectively apply fixes and correct the problem areas of the design.

Accurate calculation of RDS_{on} requires a 3D model representing all resistive elements of the structure. By calculating the distribution of potential and current density in all metal layers, vias, contacts, wire bonds, and devices, engineers can obtain the most accurate RDS_{on} value, allowing them to optimize their design with confidence and deliver a predictable layout. To better understand the impact of RDS_{on} on nearby devices and vice versa, using a SPICE netlist with distributed RC model enables circuit simulation of the power ICs with distributed devices.



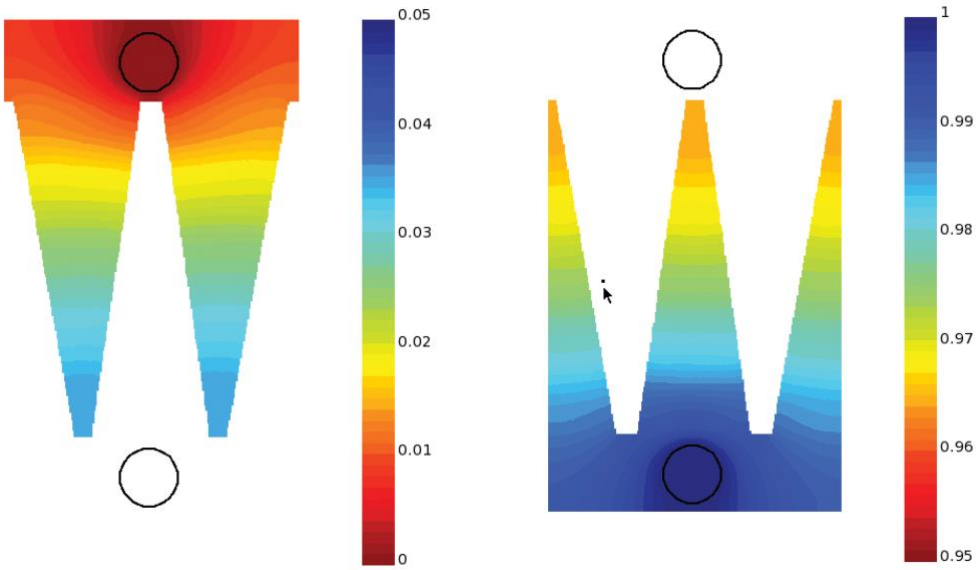
Resistance components that make up RDS_{on}

An automated way of calculating the sensitivity of RDS_{on} to individual resistive components help identify the most critical components that will effectively reduce RDS_{on}. Similarly, an automated way to decompose the total RDS_{on} value into device resistance and interconnect resistance help engineers focus on the area with highest impact on reducing RDS_{on}.

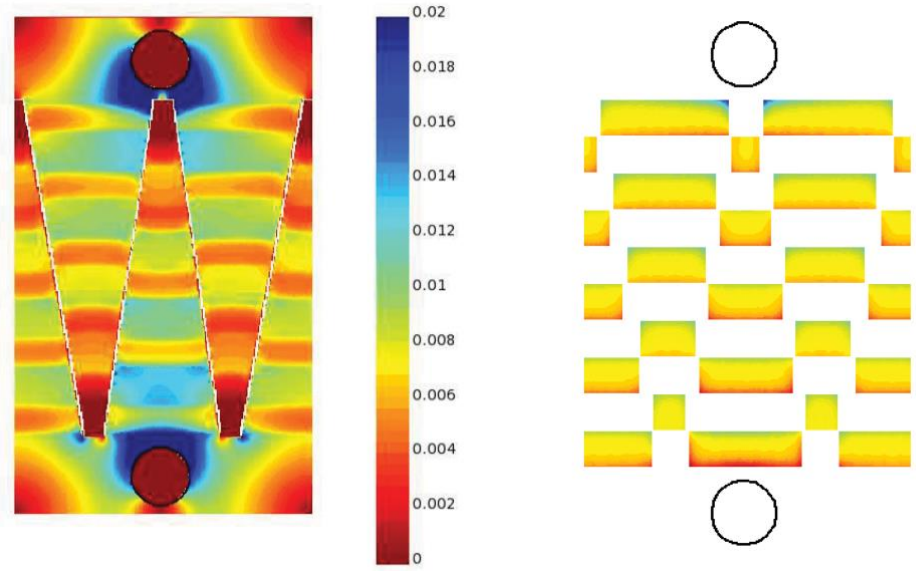
Current Density and Potential Distribution Impact on EM

Analysis of current and potential distributions allow for engineers to gain better physical insight into device operation and provide a visual aid to explore and optimize layouts and interconnects. Potential drop and current density analyses easily highlights design bugs or errors and provides a guideline for metal and via layout optimization. Access to current flow information allows engineers to optimize design slotting, reducing RDS_{on}, lowering current density, and avoiding hot spots.

High current density can cause electromigration (EM) and electro-thermal issues. In addition, heating of the die can affect RDS_{on}. Automatic identification of regions with high current densities, along with visualization of the location on the layout help improve design robustness for electromigration and electro-thermal problems.



Potential distribution of top metal layer in the source and drain nets

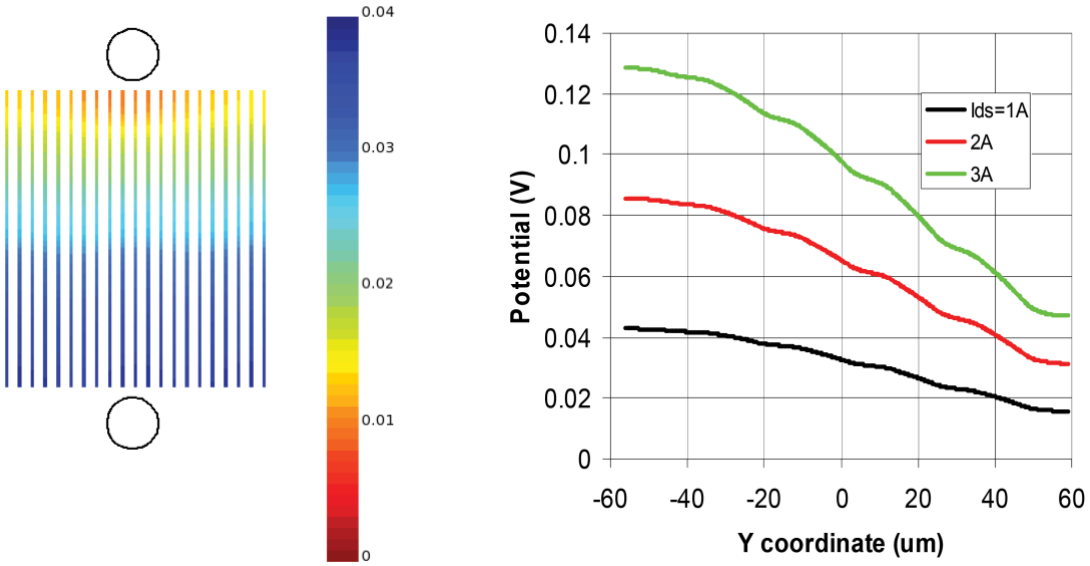


Current density distribution of top metal layer and via2

These distribution analyses allow a better physical insight into device operations, provide visual aid to explore and optimize layout interconnects.

Sense Current Device Location

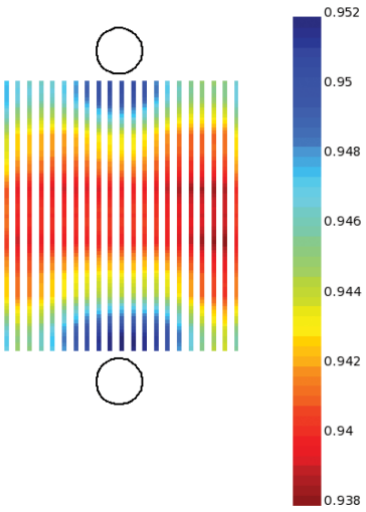
Current sense devices provide important performance feedback on how the system is operating. Optimal placement of current sense device can help improve the efficiency and reduce the risk of power loss in a design. Simulating potential distribution in source net for different current levels can help identify optimal placement for sensing transistor to provide current-independent matching.



Potential distribution in source net and its 1D cross-section for different current levels can be used to easily identify the points in M1 and M2 layouts for measuring or sensing large area device current.

Optimization for Balanced Design

Designs with balanced current distribution delivers better efficiency and higher reliability. The uniformity of current distribution is controlled by metal and via layouts, as well as the topology of the source/drain wirebonds. Non-uniform current density or current crowding in vias can result in an unbalanced design and impact RDS_{on} value. Analysis of Vds and Ids distributions over the device area provides both qualitative and quantitative estimate on balance of the design and guide engineers on required layout fixes.

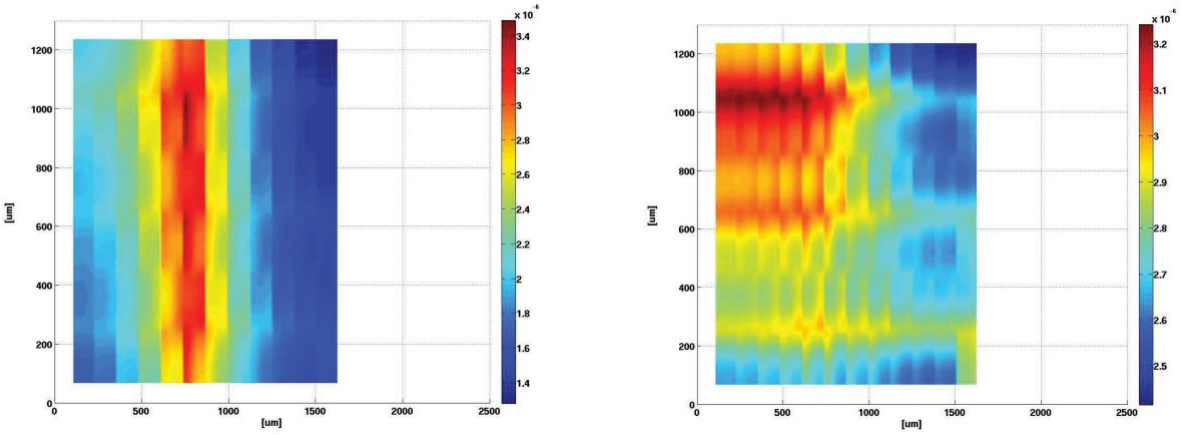


Distribution of Vds (and Ids) over the power device area provides qualitative and quantitative estimate on design balance.

Fast Turn-Around Performance and What-if Analysis

A solution with fast turn-around time allows engineers to perform "what-if" analysis to optimize the layout and explore RDS_{on} sensitivity to individual resistance component. The ability to read in standard layout files (GDSII) and technology files simplifies and speeds up the simulation process setup, as well as minimizes the possibly of human error.

A robust visualization tool helps engineers quickly inspect the plots for potential and current density distribution and immediately identify layout problems such as discontinuities, current crowding, and excessive potential drop. Ability to analyze, visualize, fix and validate quickly can help avoid schedule delays and costly silicon respins.



Visualization of Ids through device (before and after modification) shows how adding more vias between two top metal layers lead to more uniform Vds and Ids distribution over device area.

Furthermore, measurement correlations on hundreds of power devices with different layout styles, wirebonding schemes, lateral and vertical architectures, and various technology nodes ensure the robustness of a solution.

Comprehensive Analysis and Optimization Solution

A modern methodology and solution will not only manage the complexities of today's designs but will provide an environment that enable engineers to quickly identify the cause of problem area, allowing them to make corrections early in the design process and increasing their confidence in the designs efficiency and reliability.