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# FreePDK: A Free OpenAccess 45nm PDK and Cell Library for Universities

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# Goals of the FreePDK

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- Use in SRC System-on-Chip Design Contests
- Download, Distribute, and Modify Freely
  - » GNU General Public License
- Conservatively predict the performance of a commercial 45 nm technology
  - » Use 45nm Predictive Technology Model (PTM) from Berkeley/Arizona
  - » Follow the 2007 technology node in ITRS'05
- Conservatively predict functionality of a design
  - » If the FreePDK flow says “it works,” then it most likely will in a commercial flow as well
  - » Accelerate transfer of design to commercial technology
- Minimize the translation of design-data
  - » Based on OpenAccess database and Interoperable P-Cell Libraries

# NOT Goals of the FreePDK

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- NOT Intended for Fabrication
  - » could be accomplished with a greater commitment of man-months and fab-runs
- NOT Intended to control libraries or designs
  - » under GPL, derivative works must also be free
  - » libraries and designs not considered derivative works

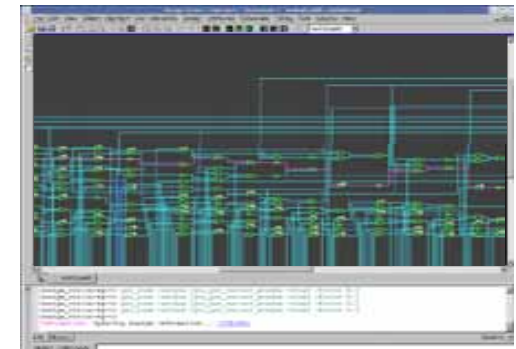
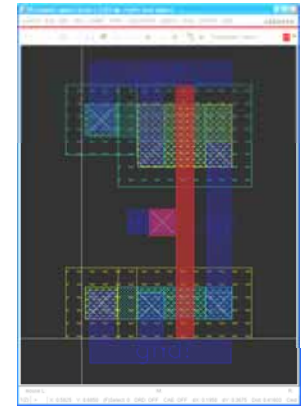
# Features of the FreePDK

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- Four NMOS, Four PMOS Devices
  - » Low, General, and High Threshold Voltage
  - » Thick Oxide
- 10 Metal Layers
- Technology Library
  - » Cadence Virtuoso 6.1.1
  - » OpenAccess 2.2.6
  - » CiraNova PyCell 4.1.1
- Calibre DRC, LVS, RC Parasitic Extraction

# Supported Design Flows

- Virtuoso 6.1.1 Layout \*
- Calibre DRC \*
- Calibre LVS & RC Parasitic Extraction \*
- HSPICE Simulation \*
- Cadabra Cell Layout
- Signal Storm Cell Characterization
- Synopsys Design Compiler Synthesis
- Encounter
- PrimeTime/PrimePower Verification
- DEF Import



\* Currently in use at NCSU VLSI Design Course

# Acknowledgements

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# Visit us on the Web

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- NCSU EDA Wiki – Base Kit
  - » <http://www.eda.ncsu.edu>
- OSU VLSI Wiki – Cell Libraries
  - » <http://vcag.ecen.okstate.edu/wiki>
- ChipTalk – Discussion Groups
  - » <http://www.chiptalk.org>